2013 S-Series Intel Shark Bay

UMA/DIS Muxless Schematic
14.0"Rampage 15.6"Renegade 17.0"Ricochet

Haswell-M Dual/Quad Core SV
rPGA947 37W
Lynx Point-M PCH

REV:MV

2013-08-01

DY:No stuff
DIS_PX:Only DIS install

<Core Design>

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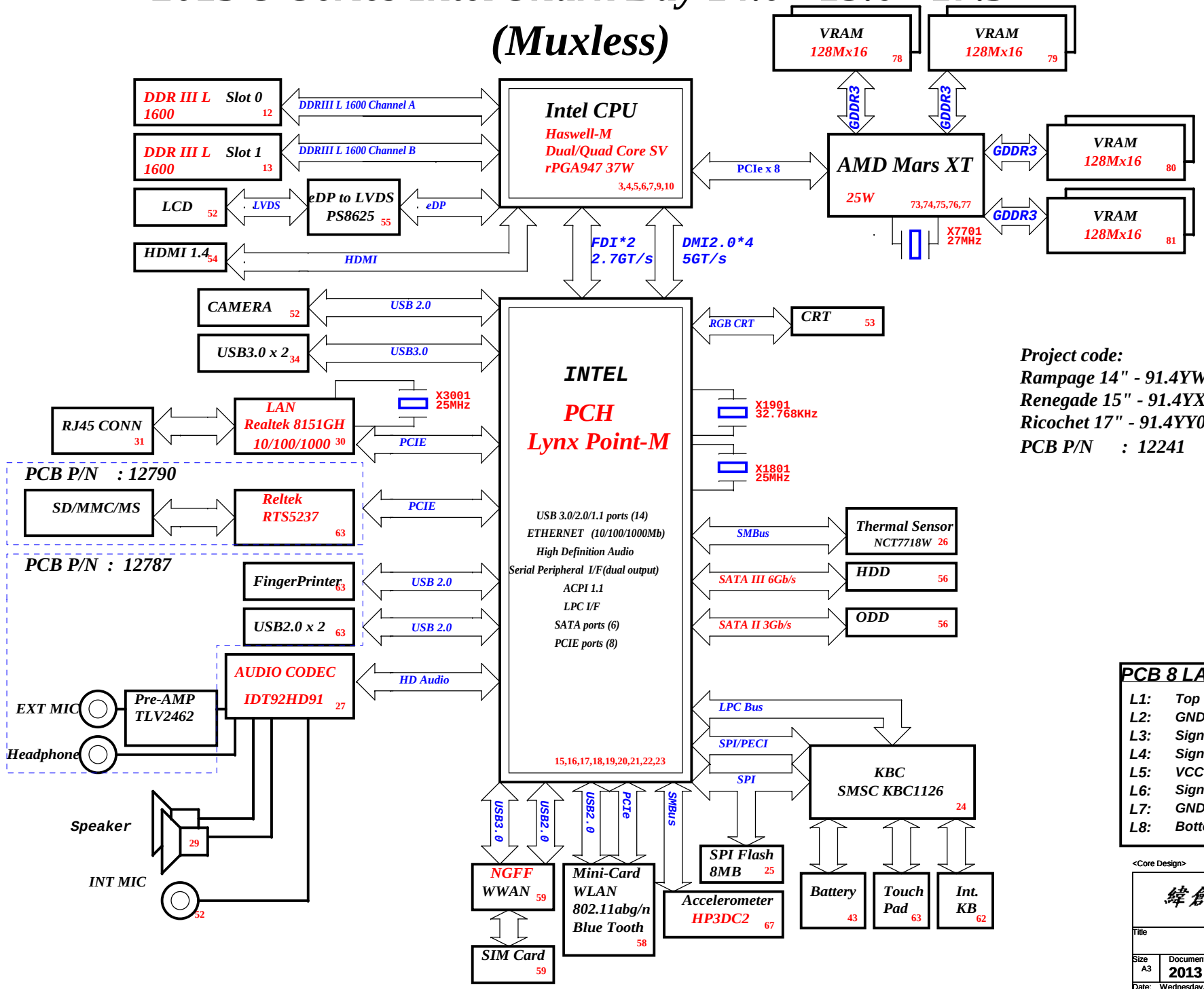
Title	***Cover Page***	
Size A4	Document Number **2013 S-Series Shark Bay 14 15 17**	Rev 1
Date: Thursday, August 01, 2013	Sheet 1 of 103	

2013 S-Series Intel Shark Bay 14.0" 15.6" 17.3" (Muxless)



Project code:
Rampage 14" - 91.4YW01.001
Renegade 15" - 91.4YX01.001
Ricochet 17" - 91.4YY01.001
PCB P/N : 12241

PCB 8 LAYER

L1:	Top
L2:	GND
L3:	Signal
L4:	Signal
L5:	VCC
L6:	Signal
L7:	GND
L8:	Bottom

CPU DC/DC TPS51631RSMR 46,47

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51367RVER 48

INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8223MZQW 45

INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS51216RUKR 49

INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0 DDR_VREF_S3

SYSTEM DC/DC APL5930KAI 51

INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

VGA ADP3211MNR2G 82

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24736RGRR 44

INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

VGA G9661-25ADJF11U 83

INPUTS	OUTPUTS
3D3V_S0	1D8V_VGA_S0

VGA APL5930KAI 83

INPUTS	OUTPUTS
1D35V_S3	0D95V_VGA_S0

Switches 36,83

INPUTS	OUTPUTS
5V_S5 3D3V_S5 3D3V_S0	5V_S0 3D3V_S0 3D3V_VGA

VGA TPS51211DSCR

INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0 83

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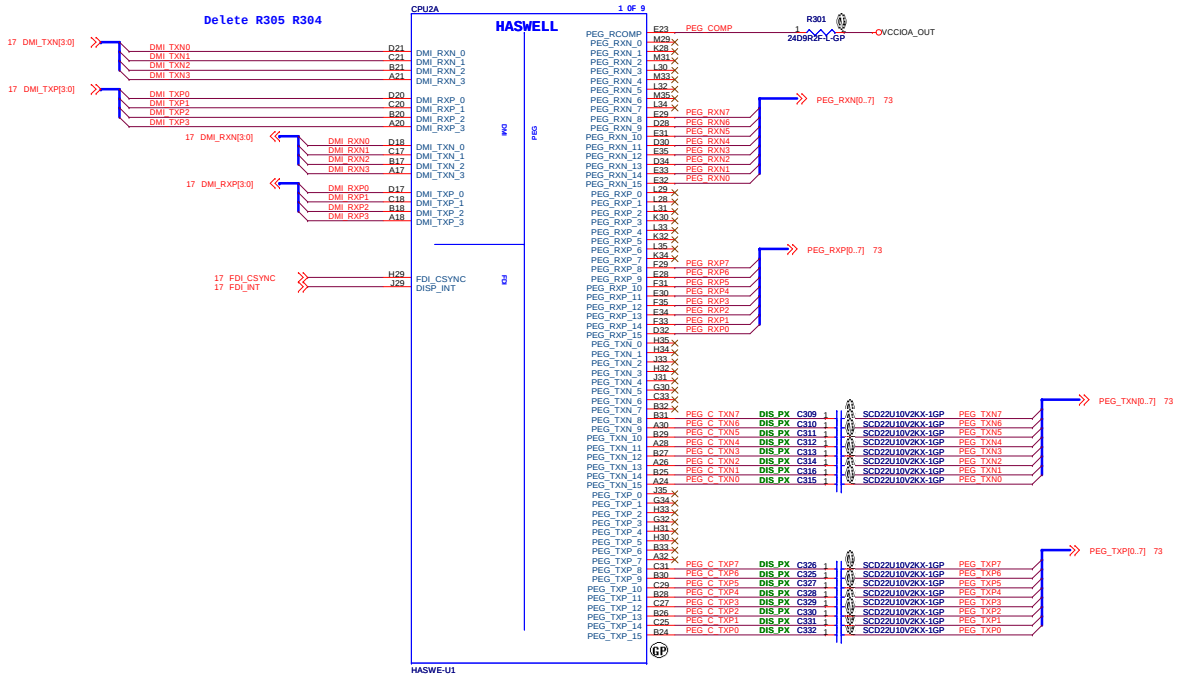
Title: **Block Diagram**

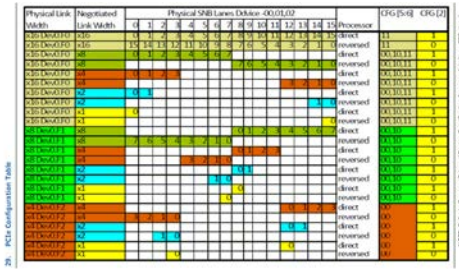
Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Wednesday, July 03, 2013 Sheet 2 of 103

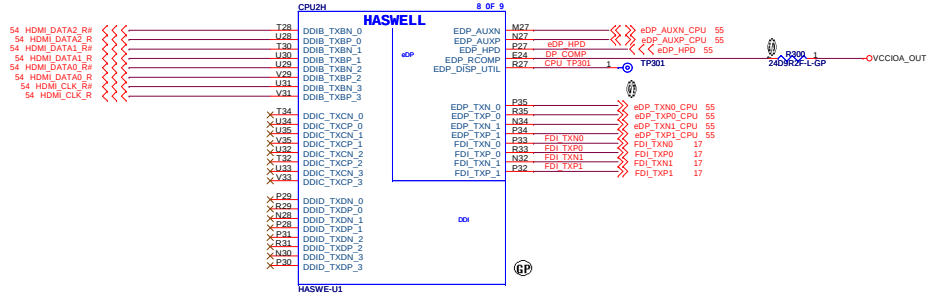
SSID = CPU

Delete R305 R304





HDMI



<Core Design>

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Title	CPU (PCIE/DMI/FDI)
Size: A2	Document Number: 2013 S-Series Shark Bay 14 15 17
Rev: 1	
Date: Monday, August 12, 2013	Sheet 3 of 103

SSID = CPU

24 KBC_PROCHOT

Q401 2N7002K-2-GP

R525 100KR2J-1-GP

H_PROCHOT#

84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

VCCIO_OUT — R401 62R2J-GP — H_PROCHOT#

1D05V_VTT — R410 100R2F-L1-GP-U — H_THERMTRIP#

1D05V_VTT — R409 0R2J-2-GP — VCCST — C401 SC1U6D3V2KX-GP

CPU2B — HASWELL — 2 OF 9

VCCST

TP401 SKTOCC# R — SKTOCC# — MISC

TP402 H_CATERR# — CATERR#

20,24 H_PECI — PECI

46 H_PROCHOT# / 20,74 H_THERMTRIP# — R413 56R2J-4-GP — H_PROCHOT# R — PROCHOT# / THERMTRIP# — THERMAL

SM_RCOMP_0 — AP3 — SM_RCOMP_0 R406 — 100R2F-L1-GP-U
SM_RCOMP_1 — AR3 — SM_RCOMP_1 R407 — 75R2F-2-GP
SM_RCOMP_2 — AP2 — SM_RCOMP_2 R408 — 100R2F-L1-GP-U
SM_DRAMRST# — AN3 — SM_DRAMRST# 37 — DDR3

20 H_CPUPWRGD — R403 10KR2J-GP — 17 H_PM_SYNC — PM_SYNC
37 VDDPWRGOOD — PWRGOOD
20 BUF_CPU_RST# — SM_DRAMPWROK
PLTRSTIN# — PWR

PRDY# — AR29 — XDP_PRDY# — TP410 TPAD14-OP-GP
PREQ# — AT29 — XDP_PREQ# — TP409 TPAD14-OP-GP
TCK — AM34 — XDP_TCK — TP413 TPAD14-OP-GP
TMS — AN33 — XDP_TMS — TP417 TPAD14-OP-GP
TRST# — AM33 — XDP_TRST# — TP415 TPAD14-OP-GP
TDI — AM31 — XDP_TDI — TP416 TPAD14-OP-GP
TDO — AL33 — XDP_TDO — TP414 TPAD14-OP-GP
DBR# — AP33 — XDP_DBRESET# — TP411 TPAD14-OP-GP — JTAG

XDP_DBRESET# 17,63

BPM_N_0 — AR30 — XDP_BPM0 — TP412 TPAD14-OP-GP
BPM_N_1 — AN31 — XDP_BPM1 — TP403 TPAD14-OP-GP
BPM_N_2 — AN29 — XDP_BPM2 — TP404 TPAD14-OP-GP
BPM_N_3 — AP31 — XDP_BPM3 — TP405 TPAD14-OP-GP
BPM_N_4 — AP30 — XDP_BPM4 — TP406 TPAD14-OP-GP
BPM_N_5 — AN28 — XDP_BPM5 — TP407 TPAD14-OP-GP
BPM_N_6 — AP29 — XDP_BPM6 — TP408 TPAD14-OP-GP
BPM_N_7 — AP28 — XDP_BPM7

18,87 CLK_DP_N_R — DPLL_REF_CLKN — G28
18,87 CLK_DP_P_R — DPLL_REF_CLKP — H28
18,87 CK_DP_SSC_N — SSC_DPLL_REF_CLKN — E27 — CK_DP_SSC_N
18,87 CK_DP_SSC_P — SSC_DPLL_REF_CLKP — E27 — CK_DP_SSC_P
18 CLK_EXP_N — BCLKN — D26
18 CLK_EXP_P — BCLKP — E26 — CLOCK

HASWE-U1

XDP_TCK — R412 51R2J-2-GP
XDP_TRST# — R411 51R2J-2-GP

3D3V_S0 — R402 1KR2J-1-GP — XDP_DBRESET#

1D05V_VTT — R404 51R2J-2-GP — XDP_TDO

RN4001 SRN1KJ-7-GP
CLK_DP_N_R
CLK_DP_P_R
1D05V_VTT

Buffered reset to CPU
Close CPU side

3D3V_S0 — C4001 SCD1U16V2KX-3GP

U401 74VHC1G09DFT2G-GP
73.01G09.AAH
IN B — VCC
IN A
GND — OUT Y

15,19,30,56,58,59,63,65,73,86,87,88 PLT_RST#

3D3V_S0 — R414 75R2J-1-GP — BUFO_CPU_RST#
1D05V_VTT — R418 1KR2J-1-GP
R416 43R2J-GP — BUF_CPU_RST#
R417 20KR2J-L2-GP
R415 0R2J-2-GP

<Core Design>

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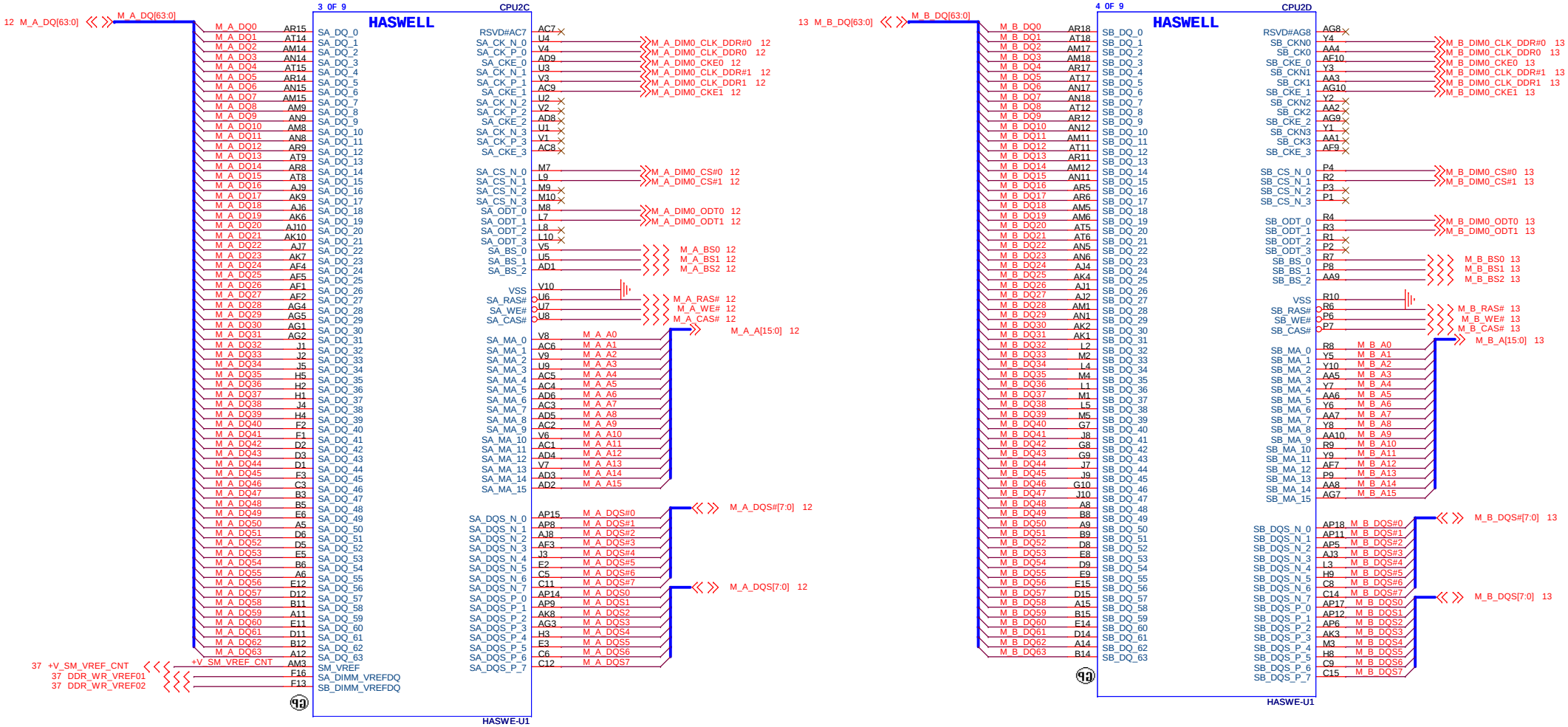
Title: ***CPU (THERMAL/CLOCK/PM)***

Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

Date: Monday, August 12, 2013 Sheet 4 of 103

SSID = CPU



<Core Design>

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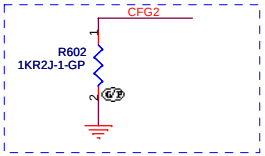
Title: ***CPU (DDR)***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

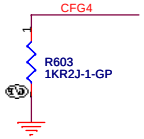
Date: Monday, August 12, 2013 Sheet 5 of 103

SSID = CPU

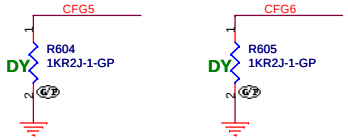
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



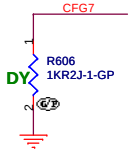
eDP Enable	
CFG4	1:Disable 0:Enable

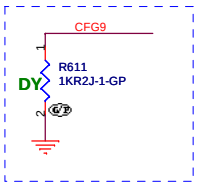


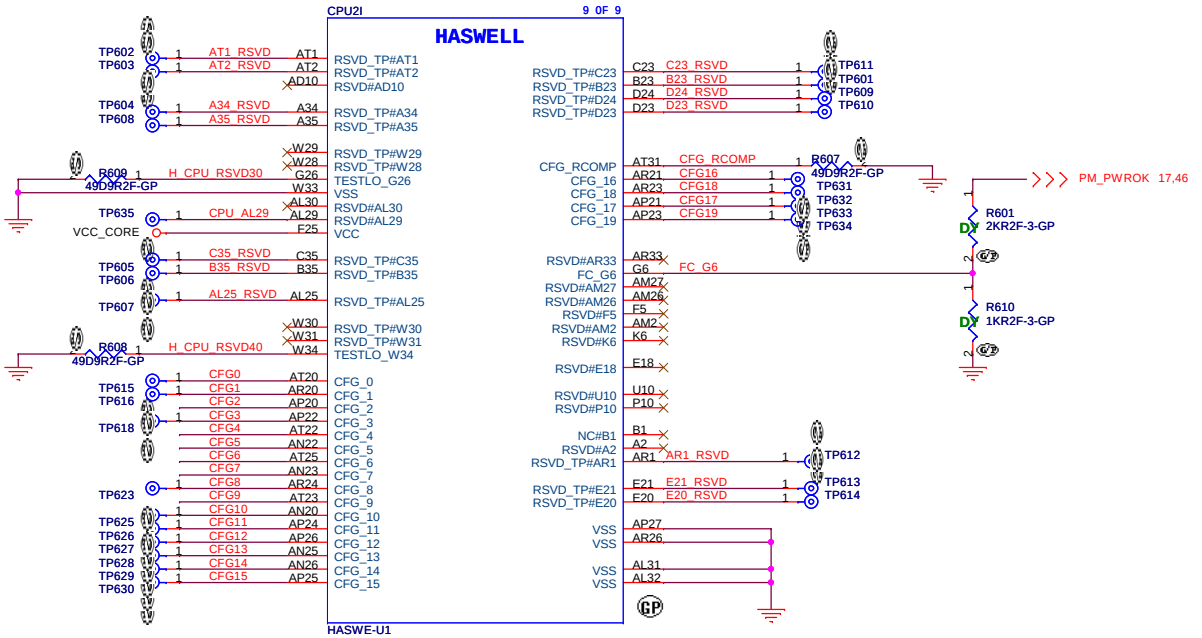
PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training







<Core Design>

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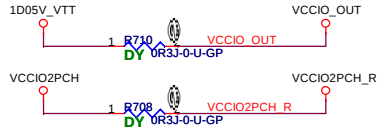
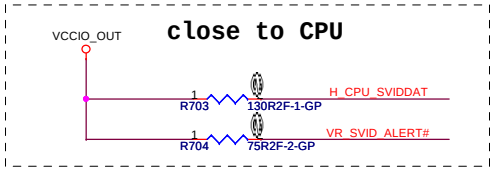
Title: CPU (RESERVED)

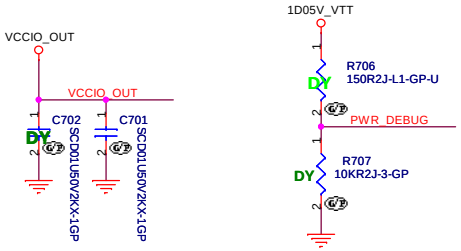
Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

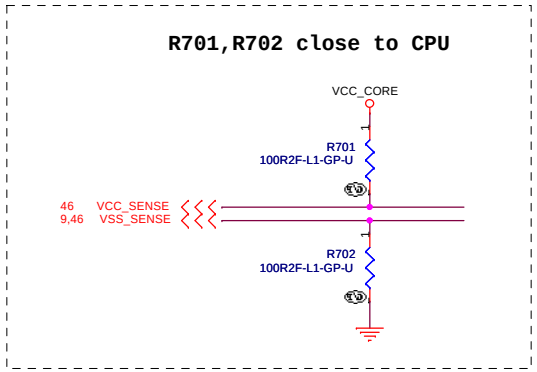
Date: Monday, August 12, 2013 | Sheet 6 of 103

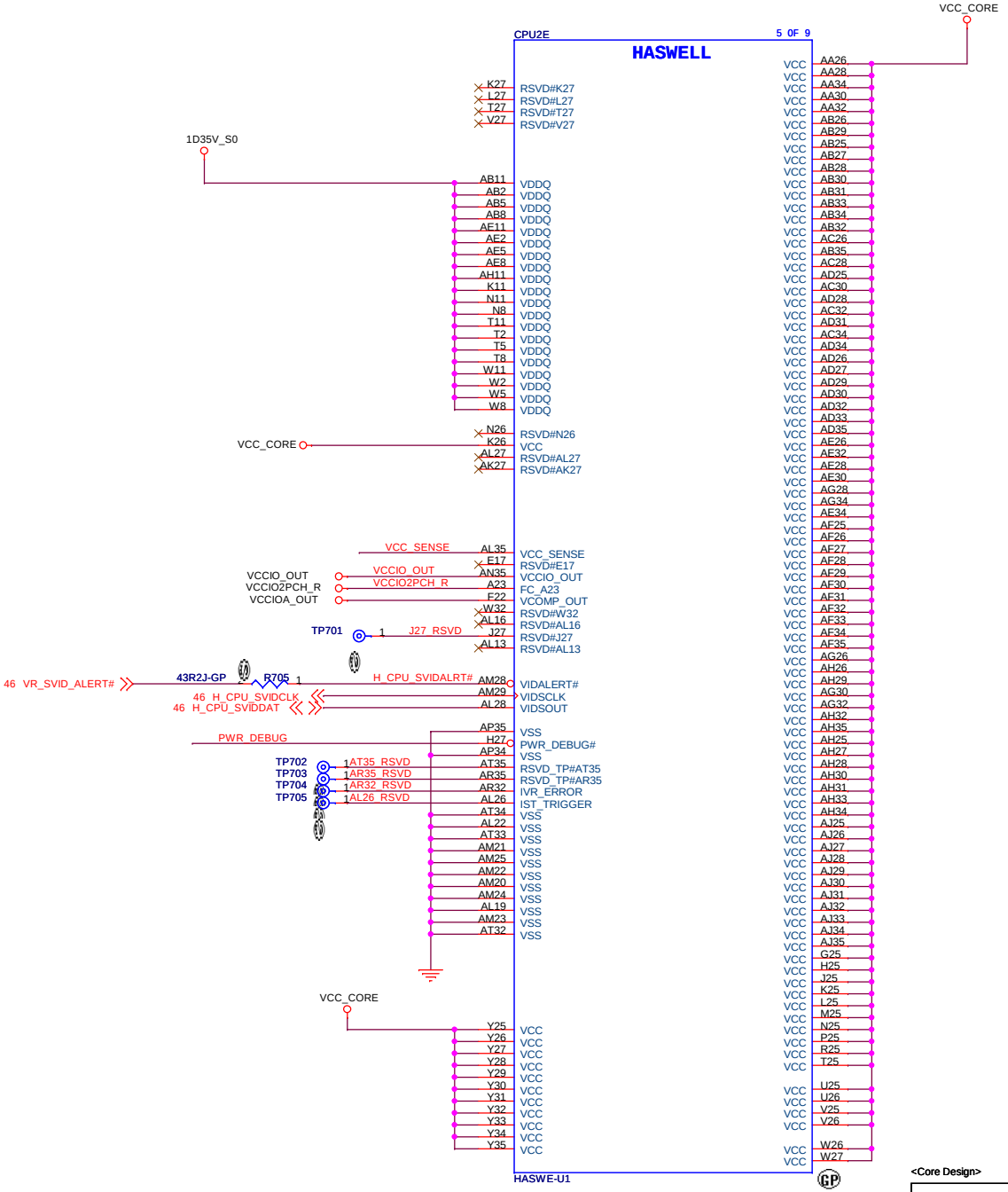
SSID = CPU











<Core Design>

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Title: **CPU (VCC)**

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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(Reserved)

<Core Design>

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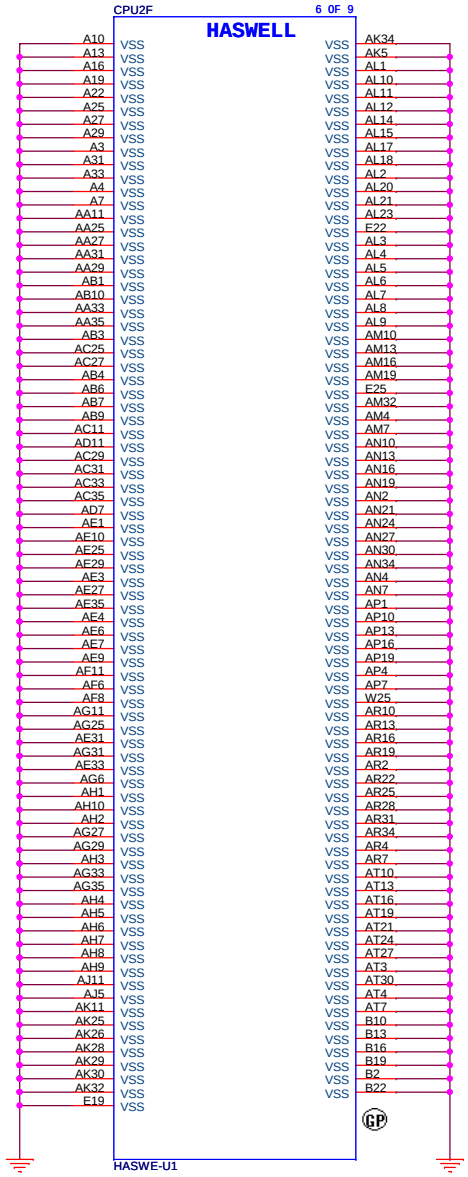
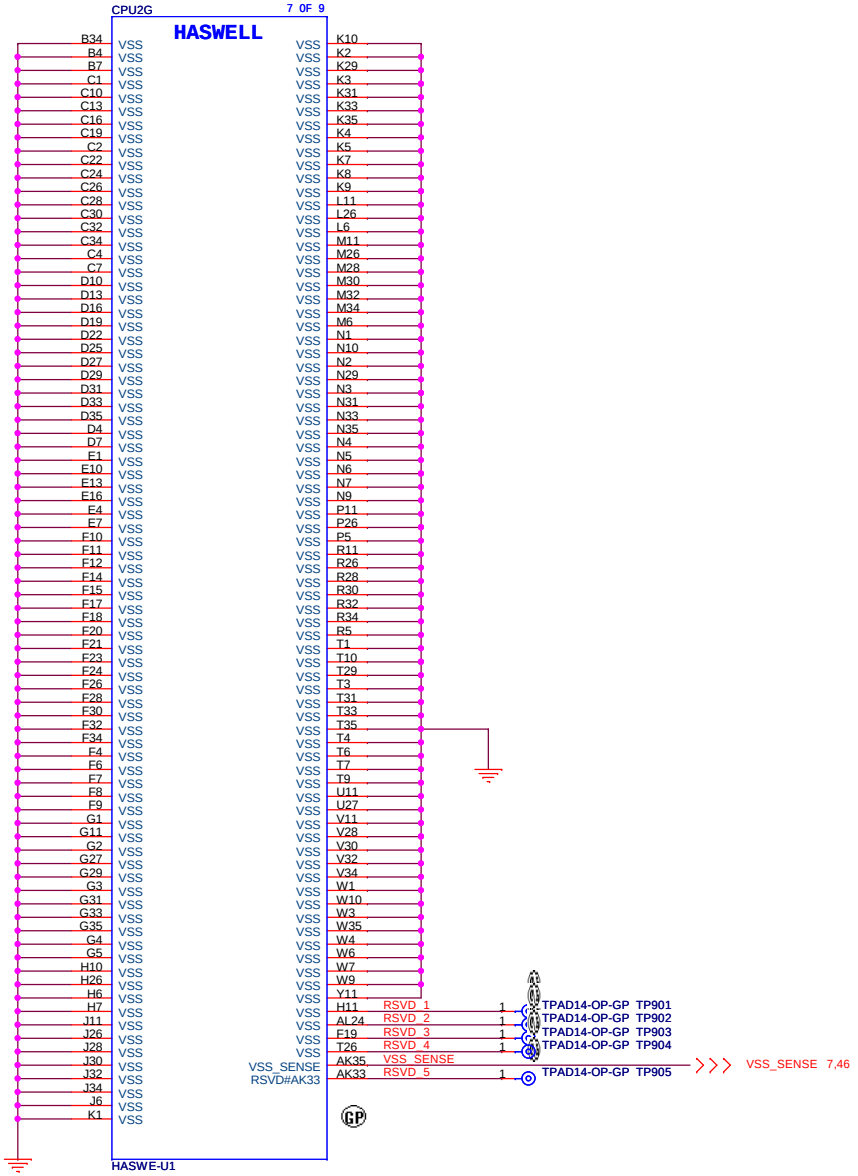
Title: *CPU (DDI/EDP)*

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

SSID = CPU





<Core Design>

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Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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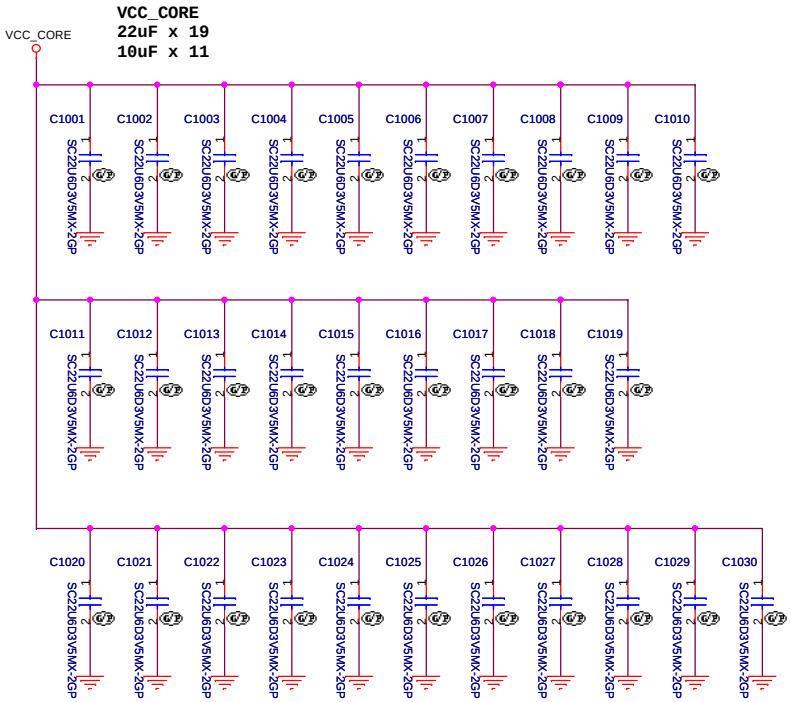

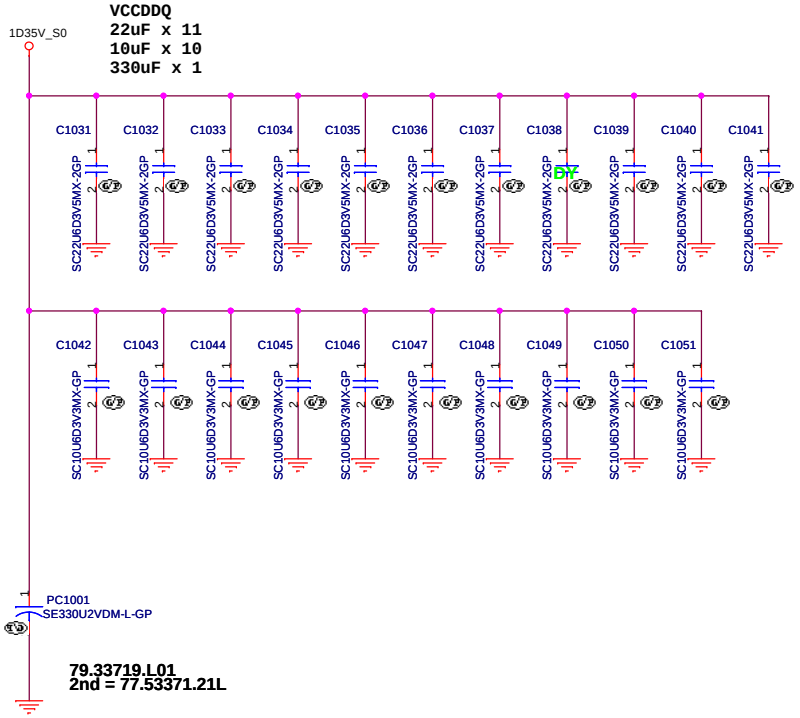

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Title: ***010 CPU (Power CAP1)***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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(Reserved)

<Core Design>

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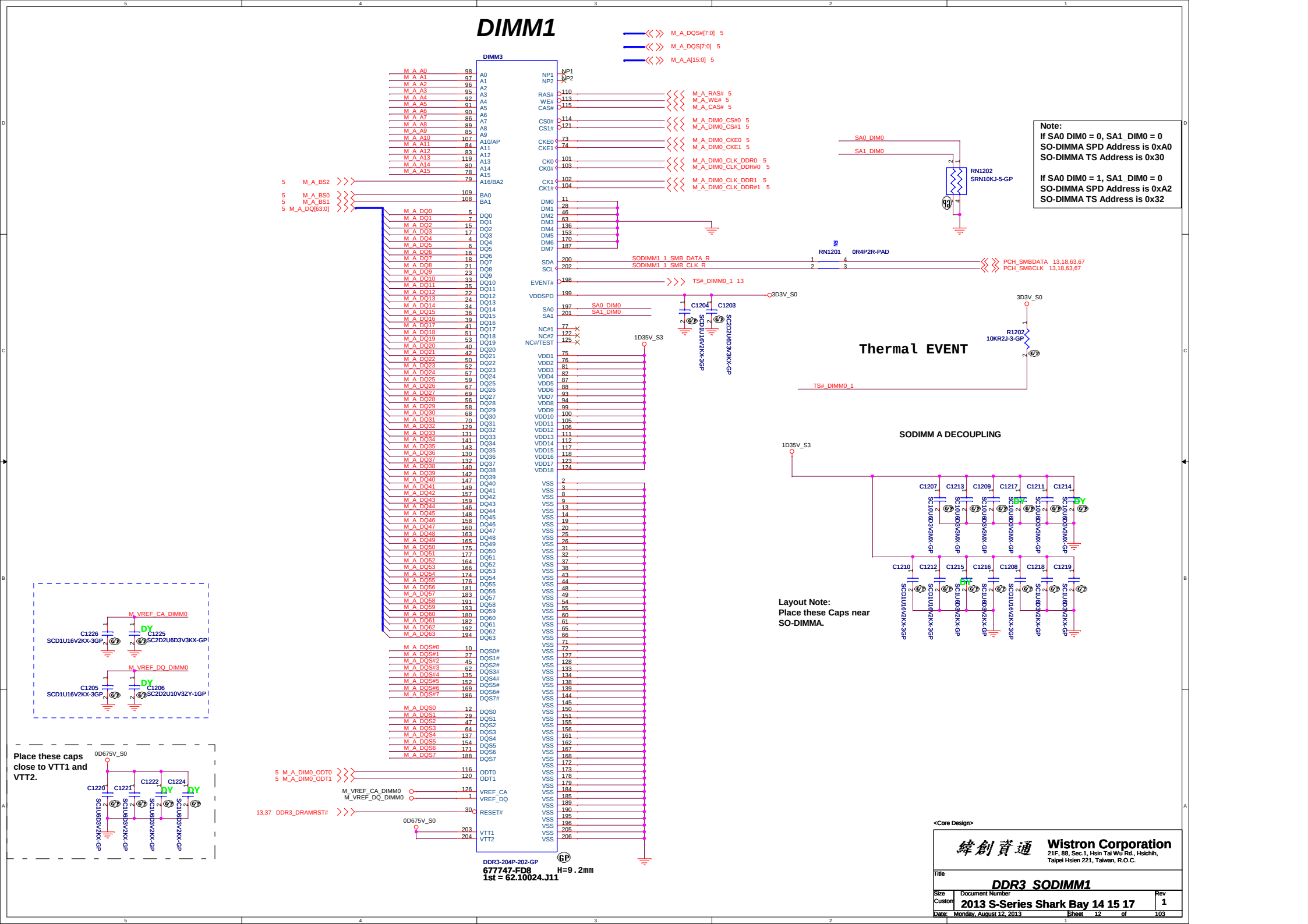
Title: *CPU(Power CAP2)*

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

DIMM1



<Core Design>

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Title: **DDR3_SODIMM1**

Size	Document Number	Rev
Custom	2013 S-Series Shark Bay 14 15 17	1

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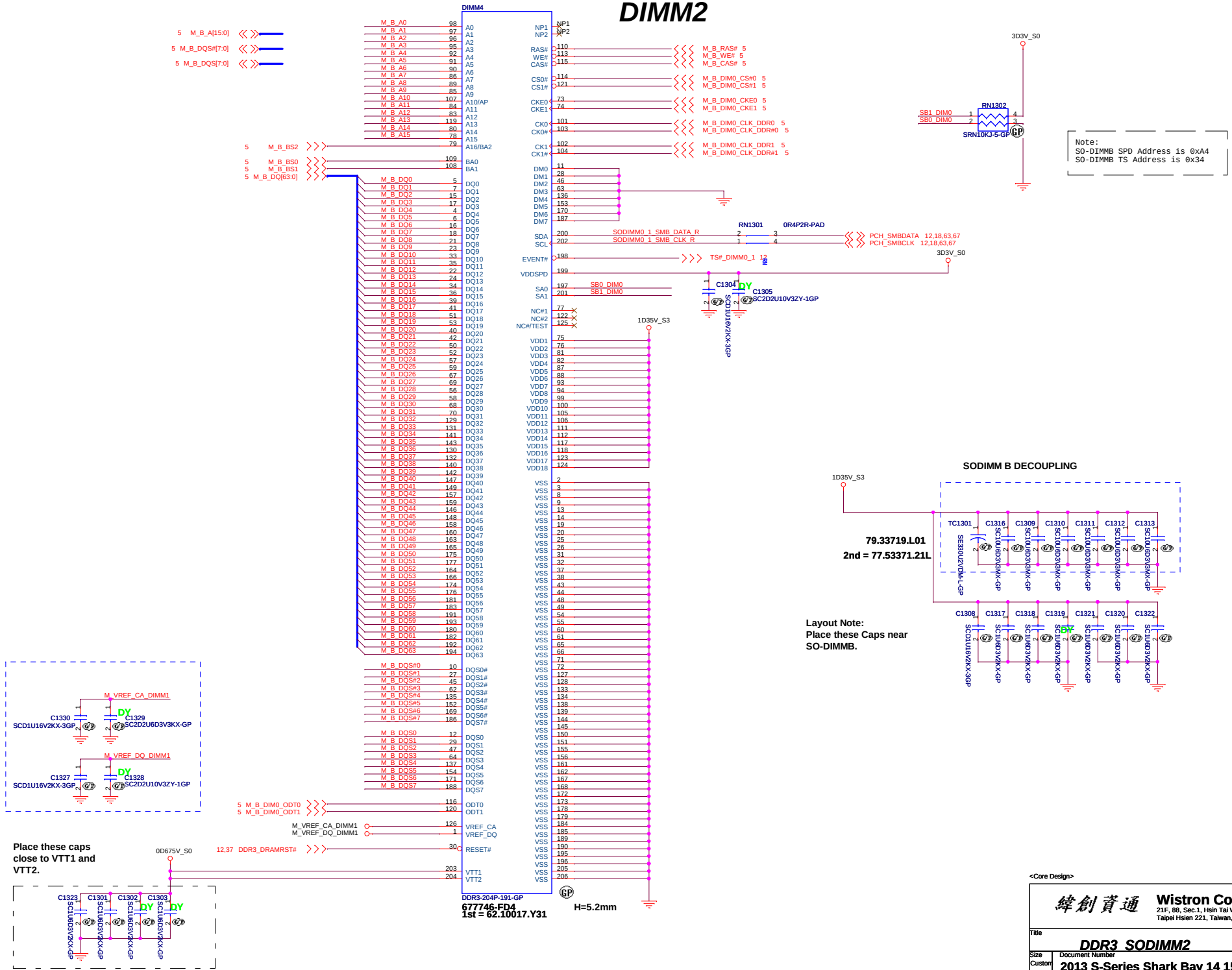
DIMM2



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

Place these caps close to VTT1 and VTT2.

SODIMM B DECOUPLING

Layout Note:
Place these Caps near SO-DIMMB.

<Core Design>

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Title: DDR3_SODIMM2

Size	Document Number	Rev
Custom	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 13 of 103

<Core Design>

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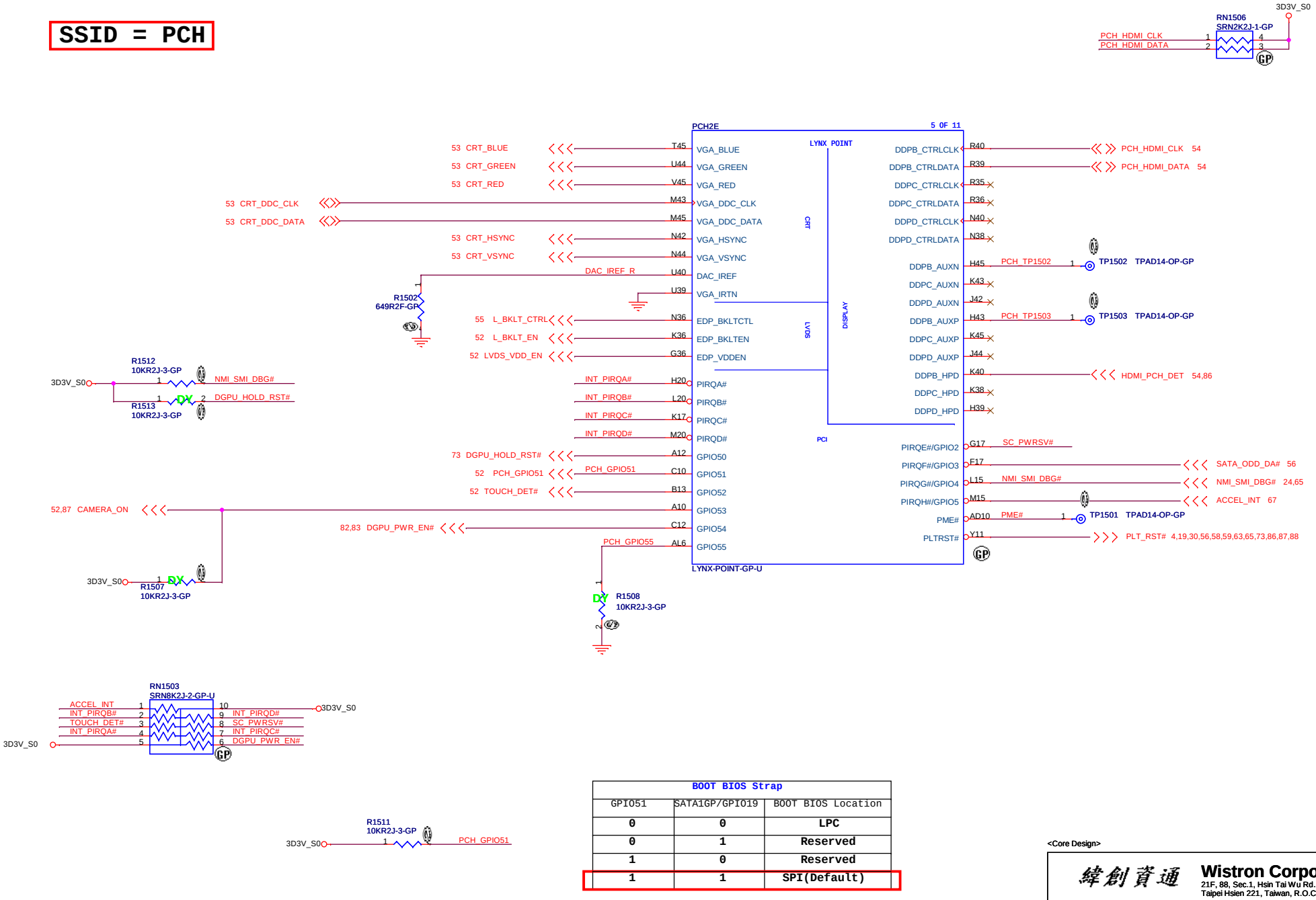
Title: ***(Reserved)SODIMM3***

Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

Date: Wednesday, July 03, 2013 Sheet 14 of 103

SSID = PCH



BOOT BIOS Strap		
GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

<Core Design>

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Title: PCH (PCI/CRT/DDI)

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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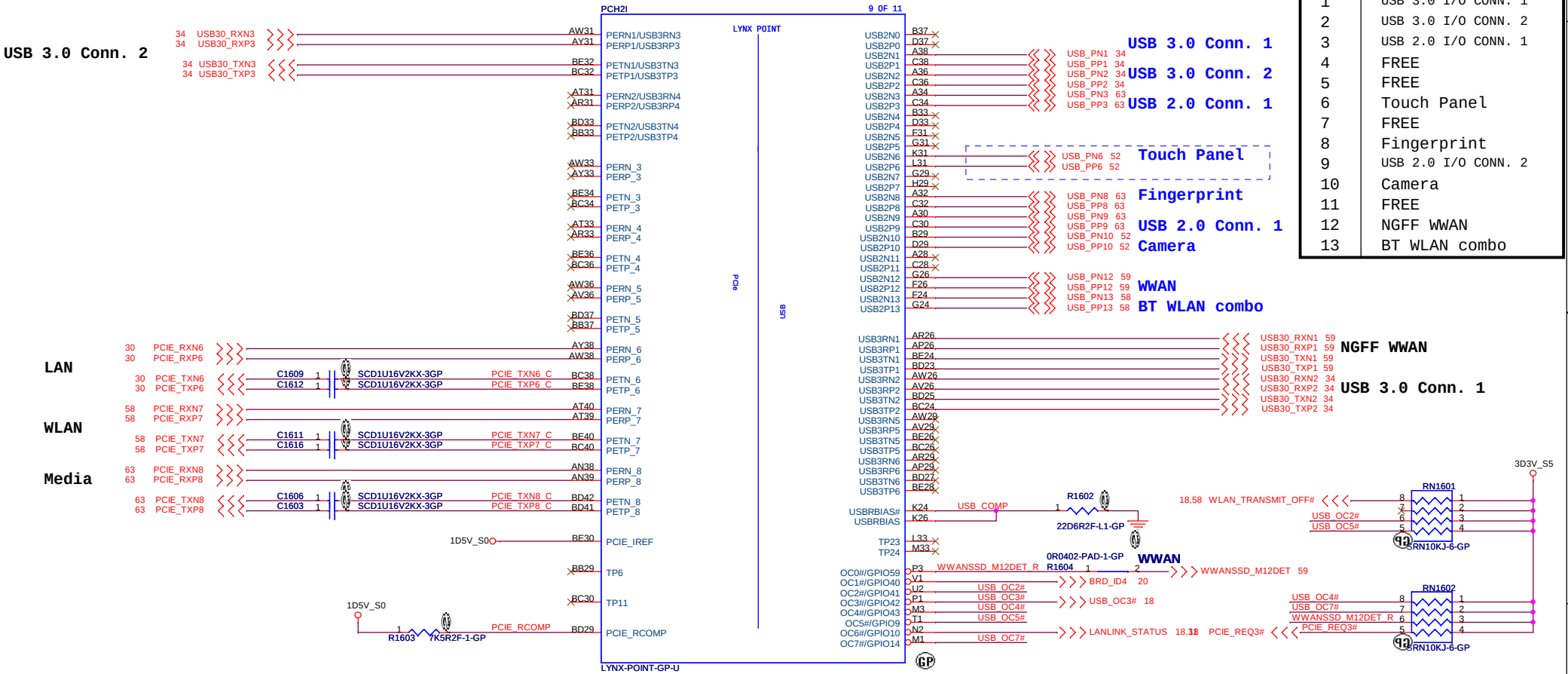
SSID = PCH

USB2.0 Table

USB	
Pair	Device
0	FREE
1	USB 3.0 I/O CONN. 1
2	USB 3.0 I/O CONN. 2
3	USB 2.0 I/O CONN. 1
4	FREE
5	FREE
6	Touch Panel
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN. 2
10	Camera
11	FREE
12	NGFF WWAN
13	BT WLAN combo



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (PCIE/USB)***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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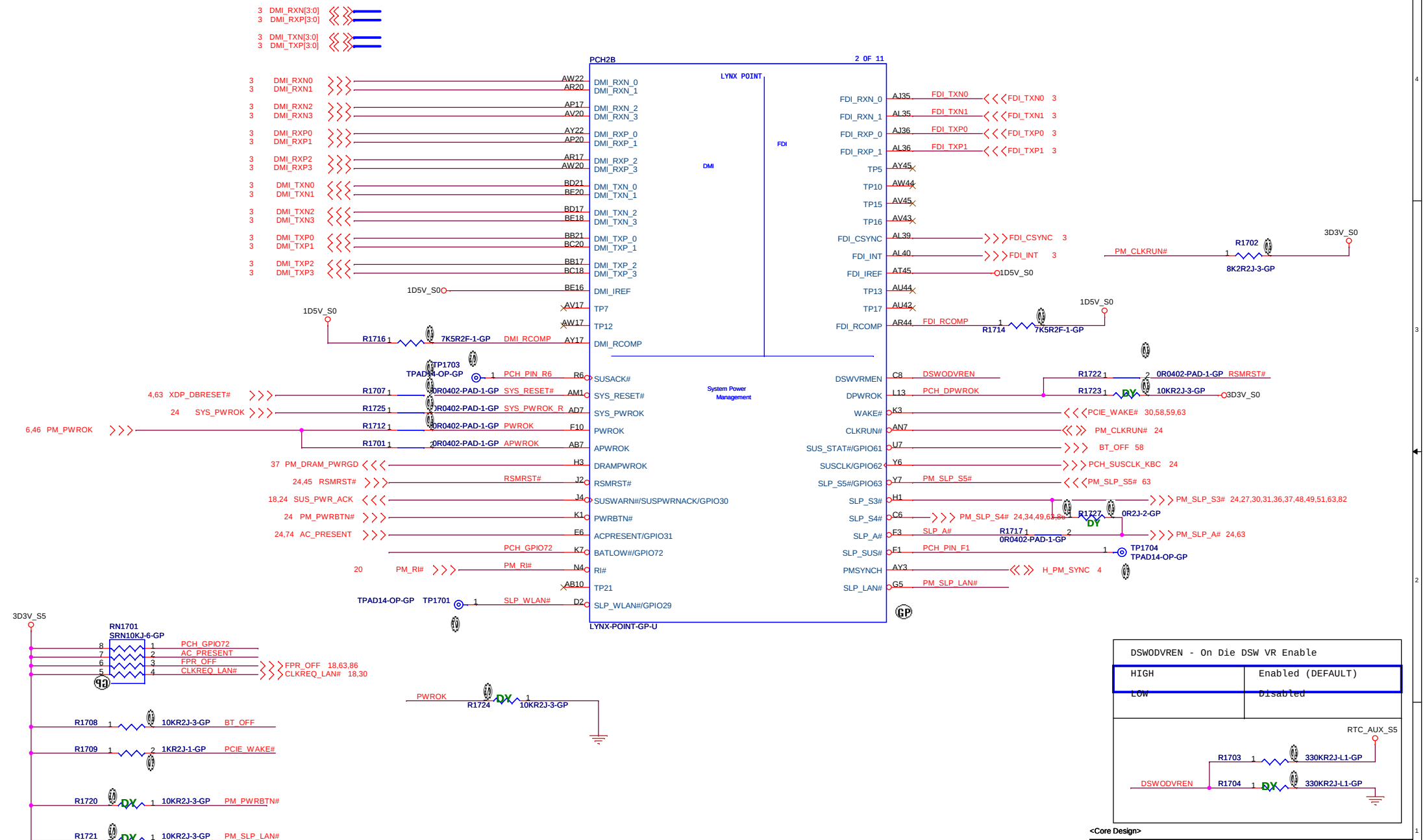
SSID = PCH



DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DMI/FDI/PM)

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 17 of 103

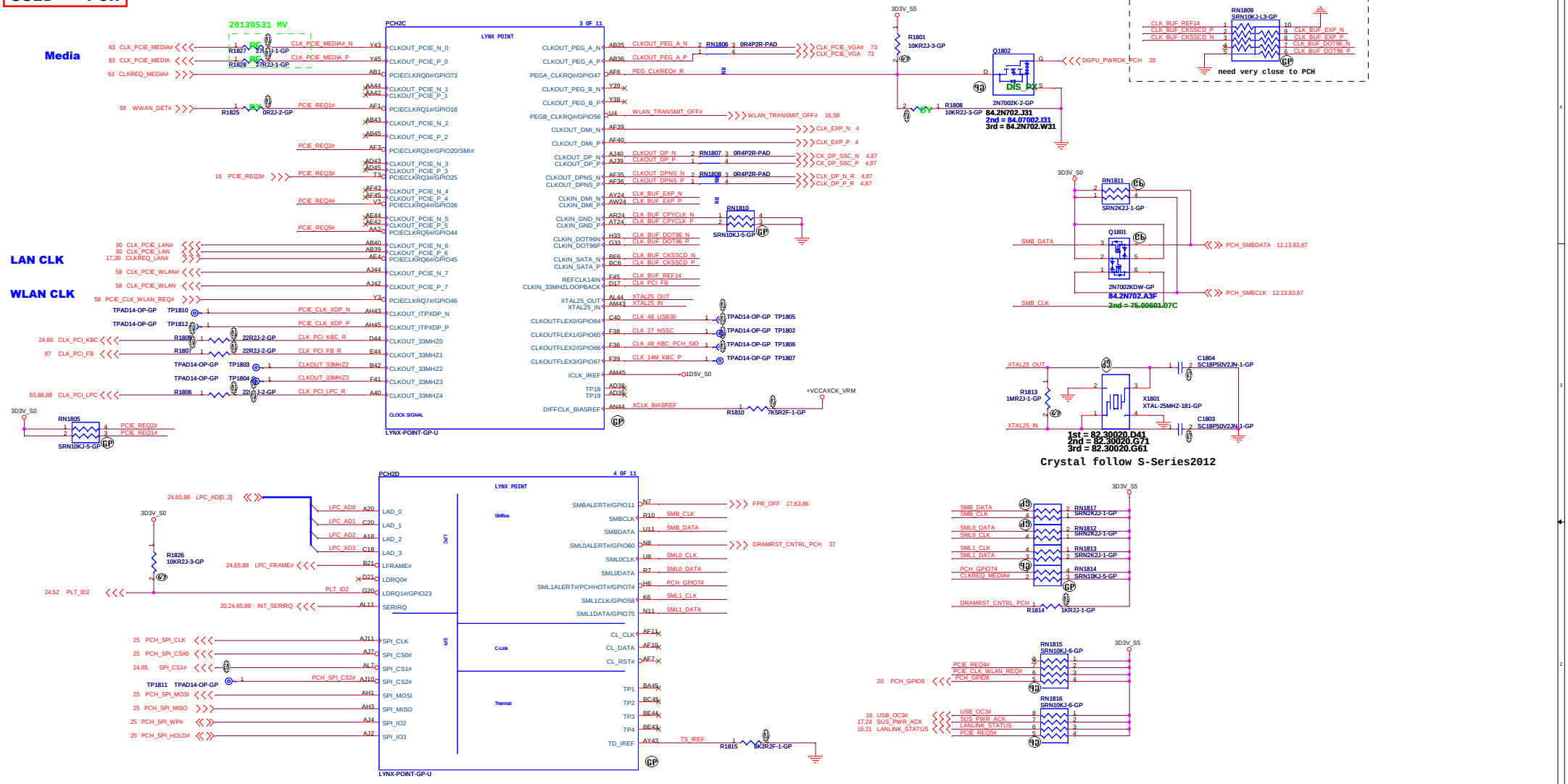
SSID = PCH

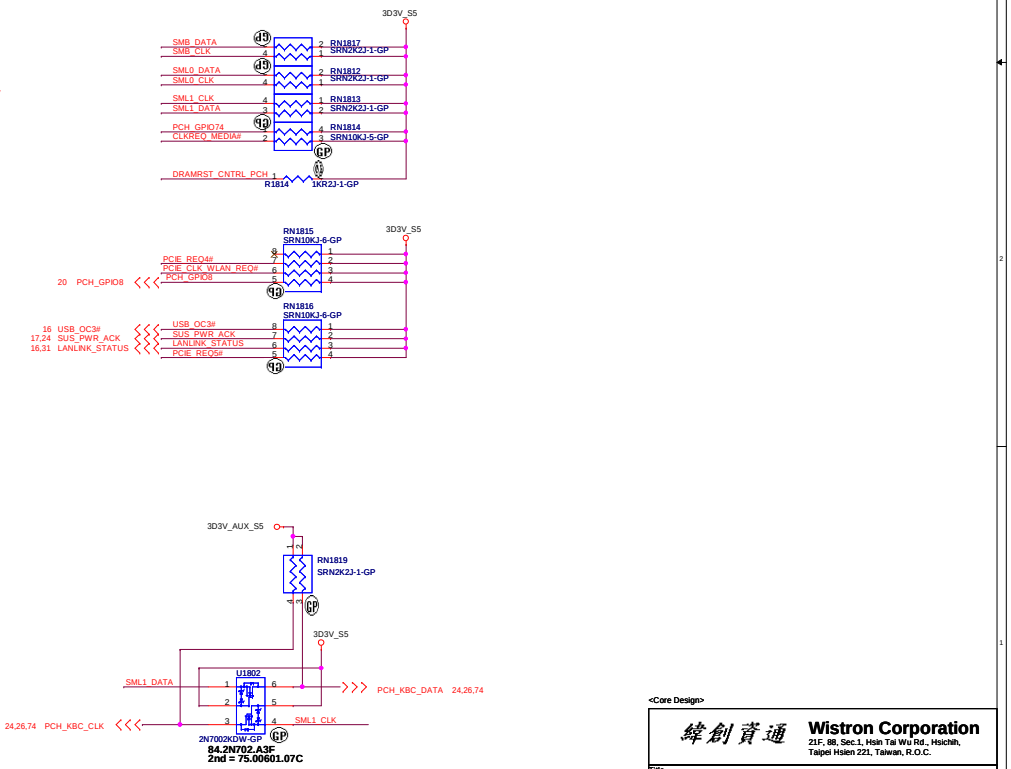
20130531 MV

Media

LAN CLK

WLAN CLK





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: A2 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 18 of 103

SSID = PCH

Close to PCH

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

HDA_SYNC:
HDA_SYNC signal also serves as a strap for selecting VRM voltage to the PCH. The strap
is sampled on the rising edge of RSMRST# signal. Due to potential leakage on the codec (path to GND), the strap may not be able to achieve the Vihmin at PCH input. Therefore, platform may need to isolate this signal from the codec during the strap phase.

<Core Design>

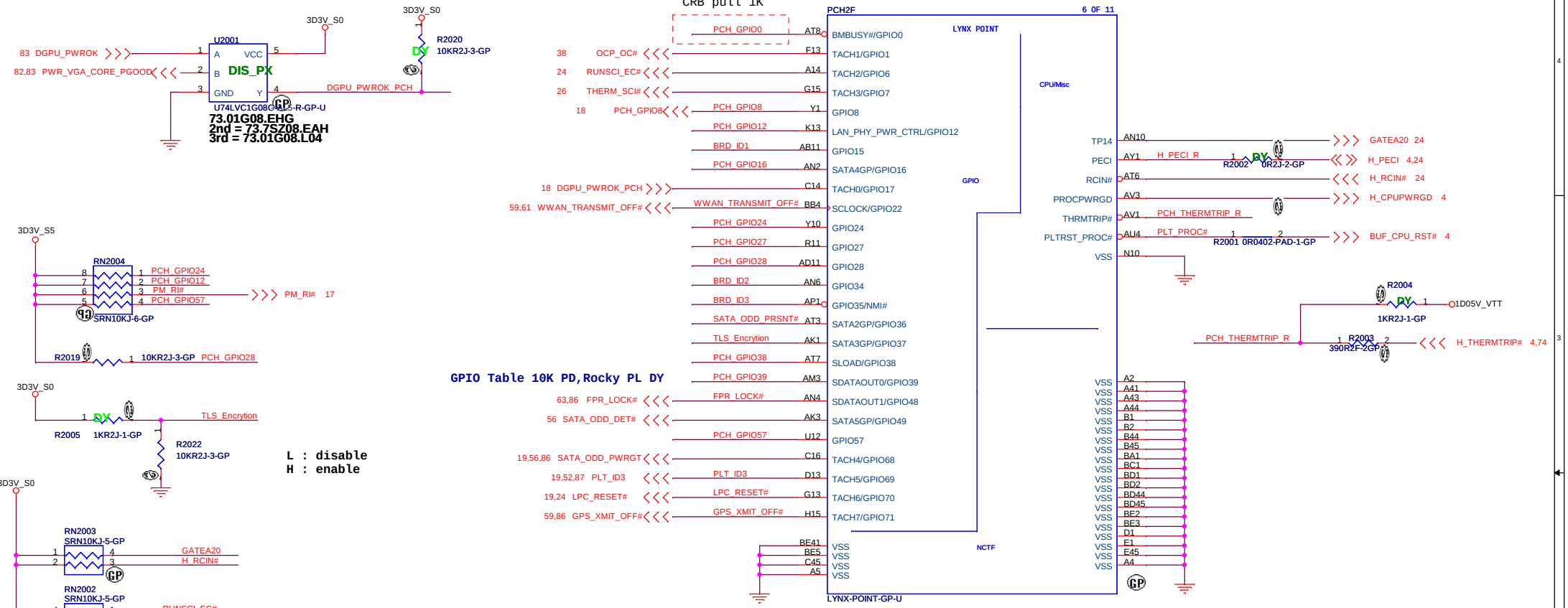
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (RTC/SATA/IHDA/JTAG)

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 19 of 103

SSID = PCH



PCH_GPIO39	PCH_GPIO38	
0	1	128MX16
1	0	N/A
1	1	UMA
0	0	64MX16

	GPIO23 PLT_ID2	GPIO69 PLT_ID3
Rampage 14"	0	1
Renegade 15"	1	0
Ricochet 17"	1	1

	BRD_ID1 GPIO15	BRD_ID2 GPIO34	BRD_ID3 GPIO35	BRD_ID4 GPIO40
DB 0	0	0	0	0
DB 1	0	0	0	1
DB 2	0	0	1	0
	0	0	1	1
SI 1	0	1	0	0
SI 1B	0	1	0	1
SI 2	0	1	1	0
	0	1	1	1
PV 1	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
MV	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1

<Core Design>

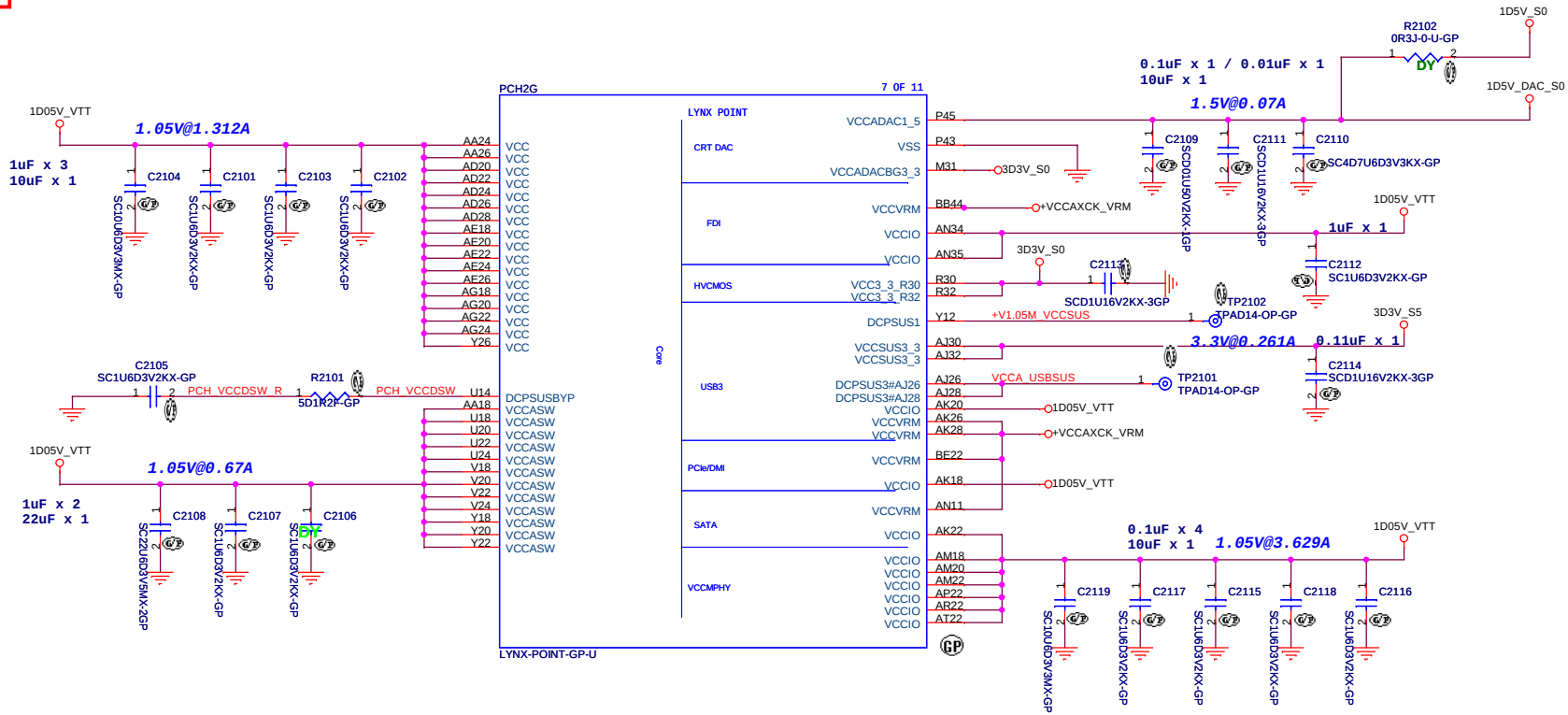
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

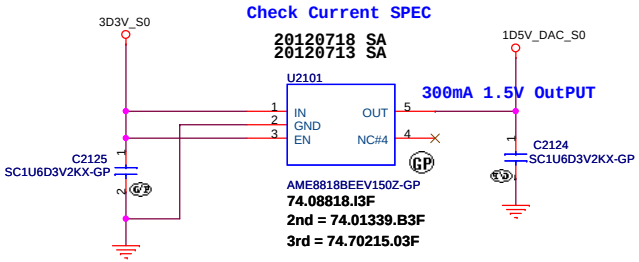
Title: PCH (GPIO/CPU)

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 20 of 103

SSID = PCH





<Core Design>

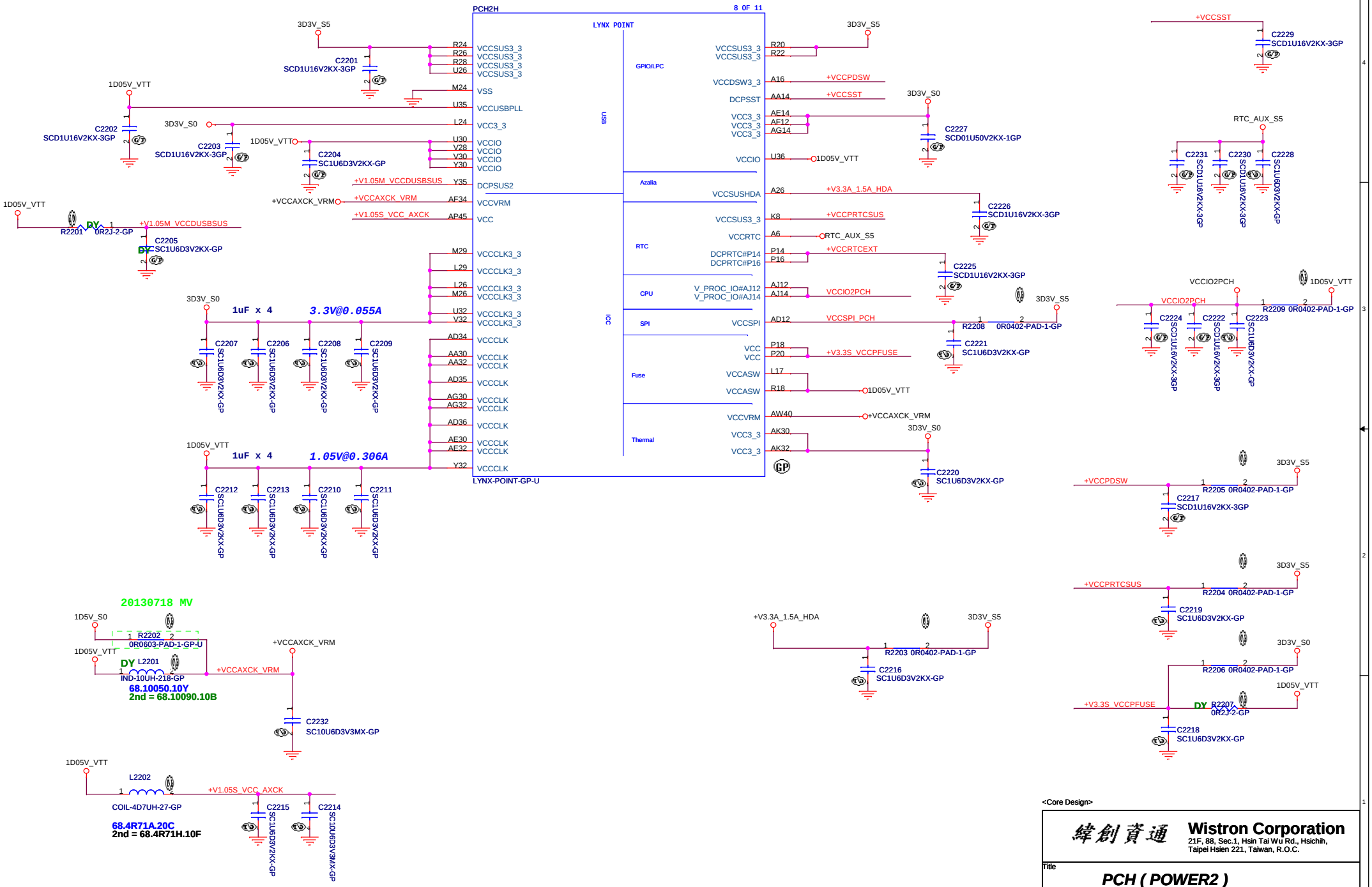
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (POWER1)***

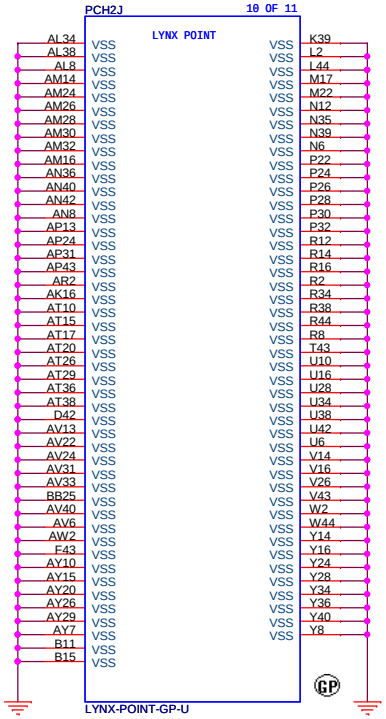
Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

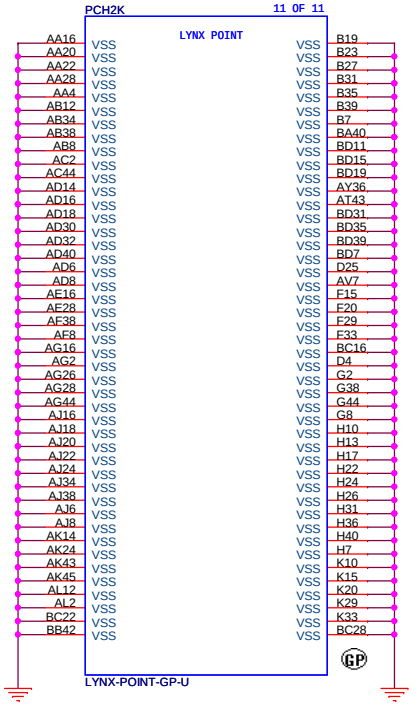
Date: Wednesday, July 24, 2013 Sheet 21 of 103

SSID = PCH


PCH2H
8 OF 11
LYNX POINT
LYNX-POINT-GP-U
GPIO/LPC
USB
Azalia
RTC
CPU
SPI
Fuse
Thermal
ICC
3D3V_S5
3D3V_S0
1D05V_VTT
1D05V_S0
+VCCSST
+VCCPDSW
+VCCPRTCSUS
+VCCPRTCEXT
+VCCSPI_PCH
+V3.3S_VCCPFUSE
+V3.3A_1.5A_HDA
+VCCAXCK_VRM
+V1.05S_VCC_AXCK
+V1.05M_VCCDUSBSUS
VCCIO2PCH
RTC_AUX_S5
1uF x 4
3.3V@0.055A
1uF x 4
1.05V@0.306A
20130718 MV
68.10050.10Y
2nd = 68.10090.10B
68.4R71A.20C
2nd = 68.4R71H.10F
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (POWER2)
Size A3
Document Number
2013 S-Series Shark Bay 14 15 17
Rev 1
Date: Wednesday, July 24, 2013
Sheet 22 of 103

SSID = PCH





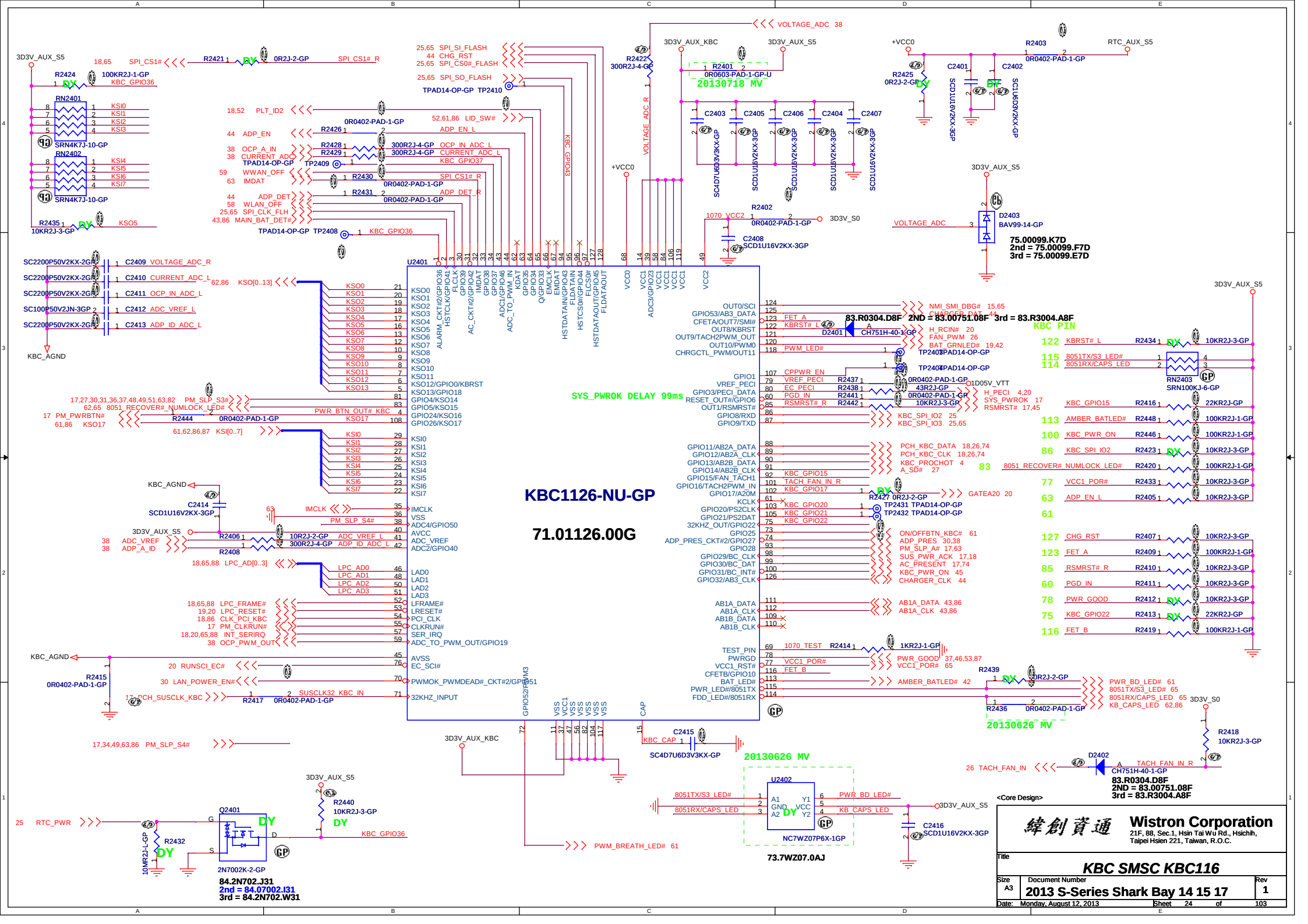
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH(VSS)***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Wednesday, July 03, 2013 Sheet 23 of 103


KBC1126-NU-GP
71.01126.00G
SYS_PWROK DELAY 99ms
U2401
U2402
83.R0304.D8F 2ND = 83.00751.08F 3rd = 83.R3004.A8F
20130718 MV
20130626 MV
75.00099.K7D
2nd = 75.00099.F7D
3rd = 75.00099.E7D
84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31
73.7WZ07.0AJ
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC SMSC KBC116
2013 S-Series Shark Bay 14 15 17
Monday, August 12, 2013

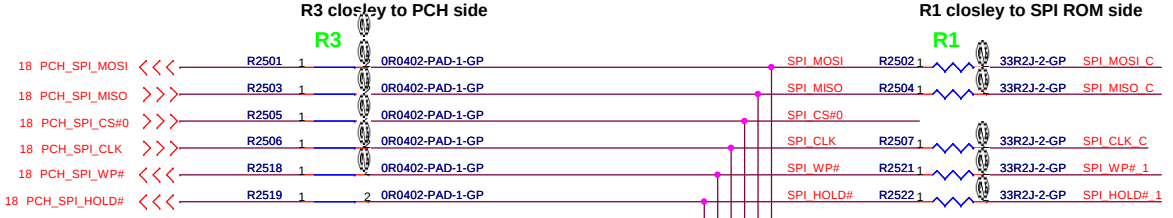
SPI FLASH ROM (8M byte) for PCH

To PCH

From BIOS

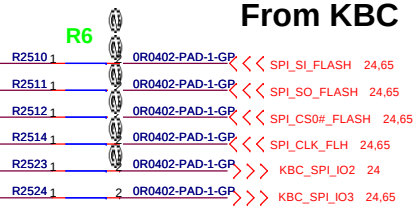
R3 closley to PCH side

R1 closley to SPI ROM side



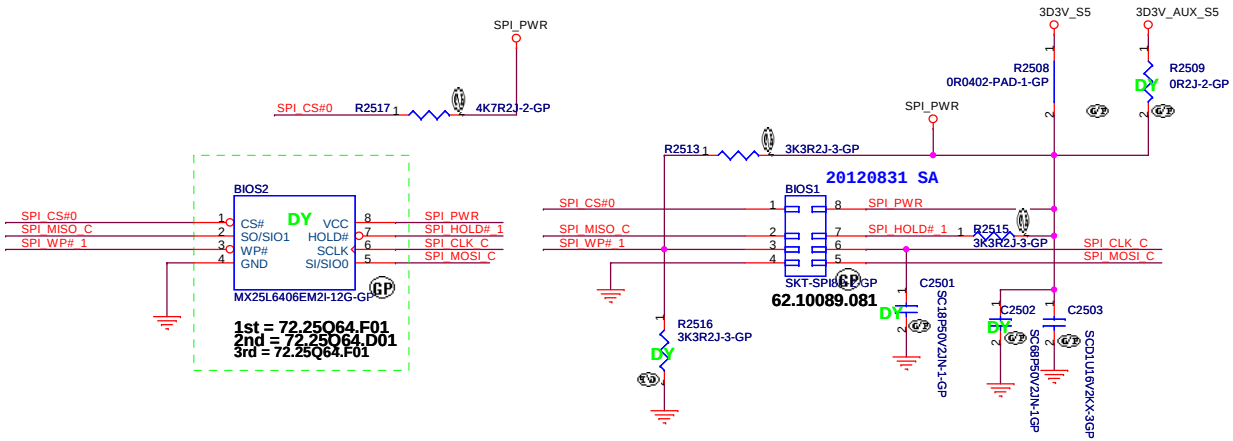
20120812 SA

From KBC



SPI_CLK — SPI_CLK 87 — To RF CAP

SYSTEM SPI ROM Socket

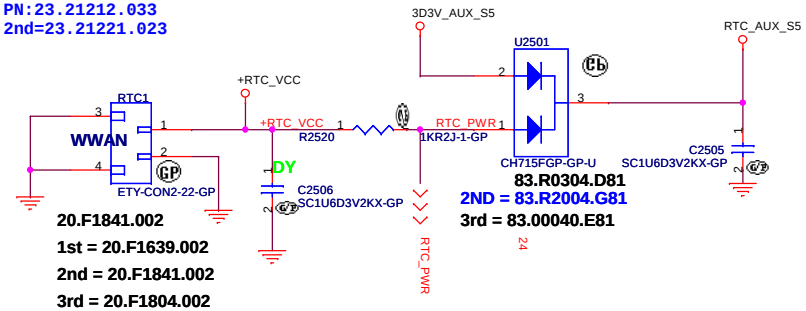


NOTE: SPI signal use GND reference

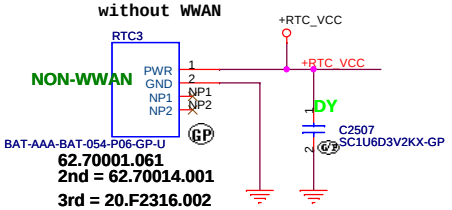
Quad IO Winbond 8M:72.25Q64.K01 (W25Q64FVSSIQ)
MXIC : 72.25647.00A (MX25L6473EM2I)
Micon: 72.25Q64.G01 (N25Q064A13ESEC0F)

RTC Battery

RTC Battery+Cable
PN:23.21212.033
2nd=23.21221.023



without WWAN



RTC Battery PN:23.22065.001
23.22063.001
23.20068.001

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

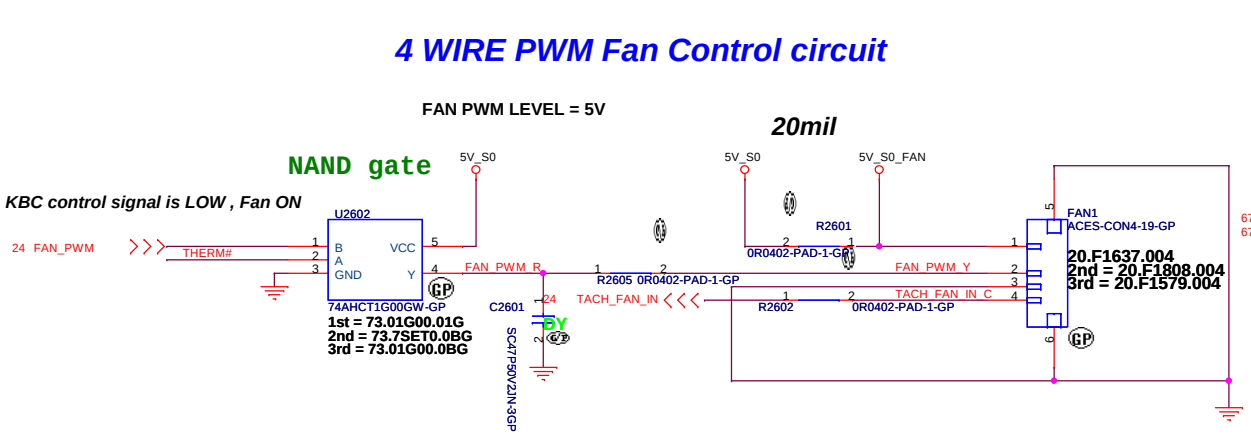
Title: Flash(KBC+PCH)/RTC

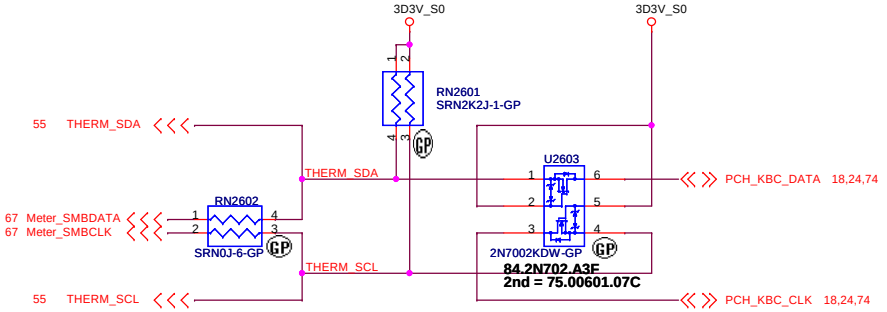
Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 25 of 103

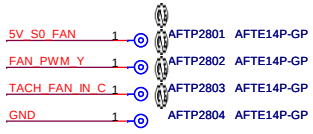
Thermal Sensor,FAN

4 WIRE PWM Fan Control circuit

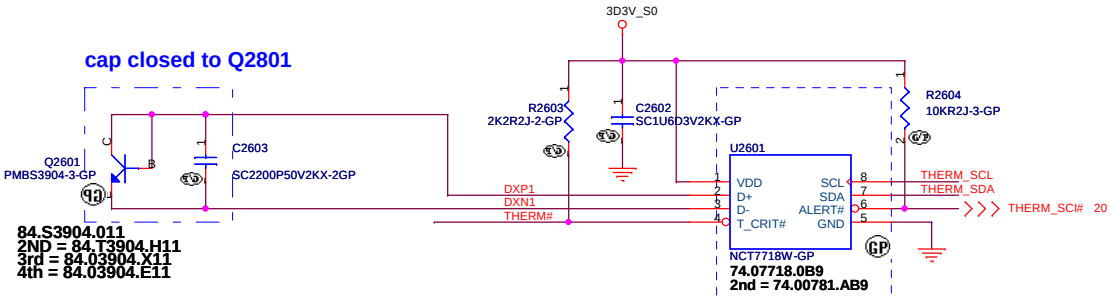




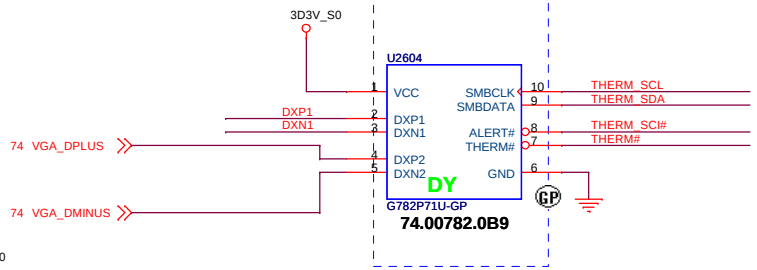
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L



Thermal IC Control circuit

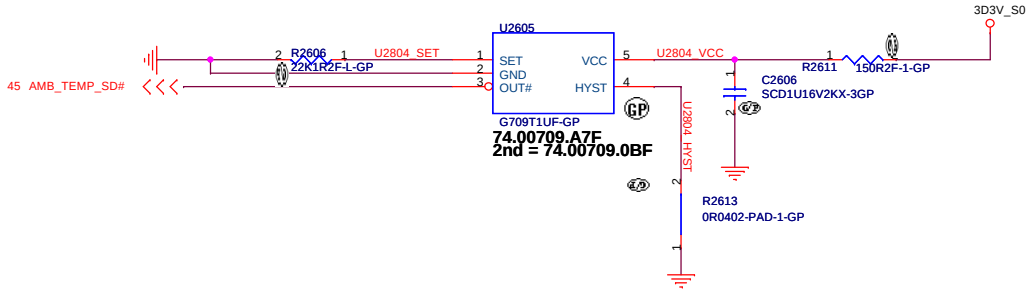


Co-Layout



T8 H/W Shutdown Control circuit

Degree	Rset
95	25.5K
90	22.1K
85	18.7K



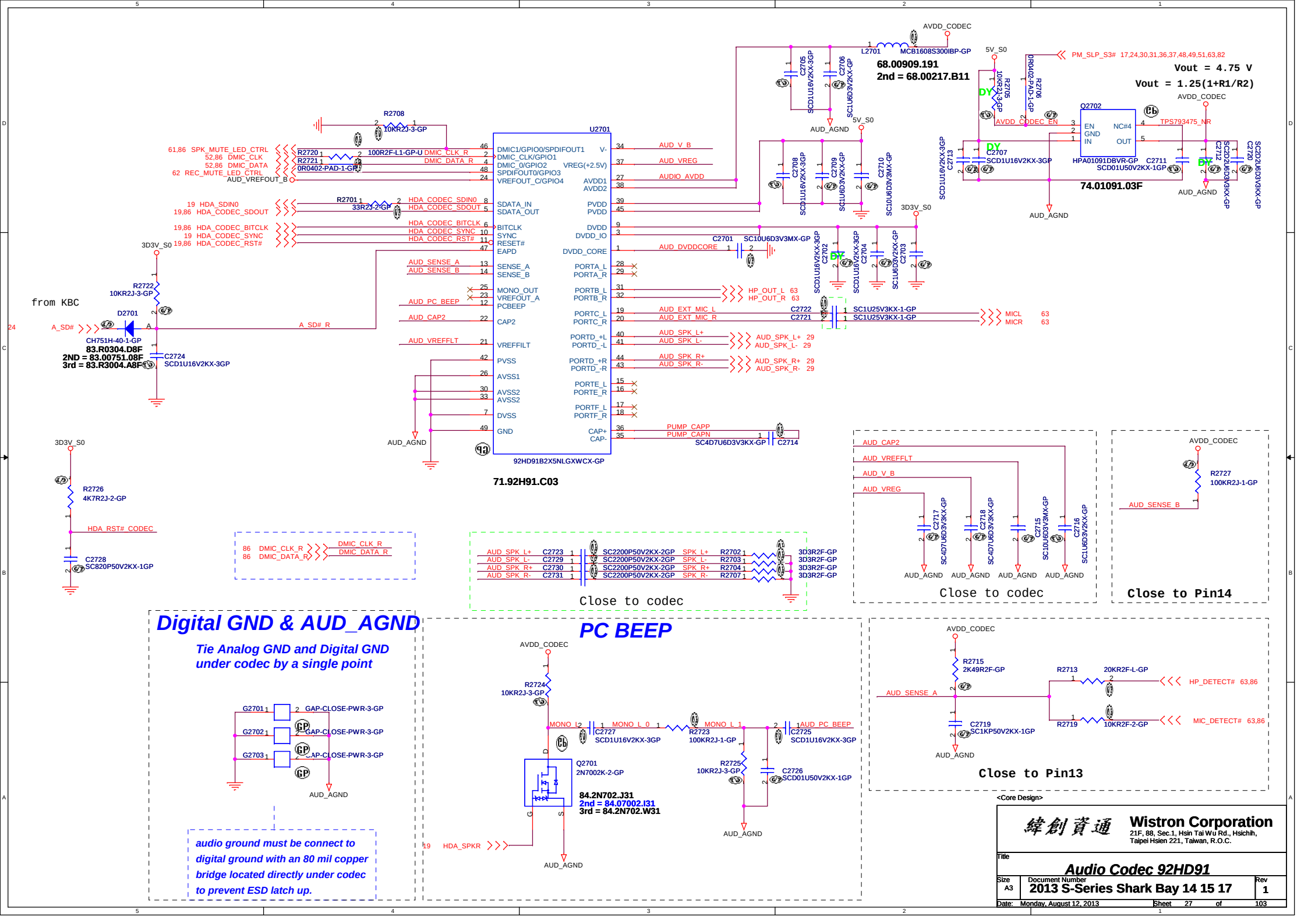
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal G781/Fan control

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 26 of 103



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<core_design>

Title: Audio Codec 92HD91

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 27 of 103
</core_design>

<Variant Name>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

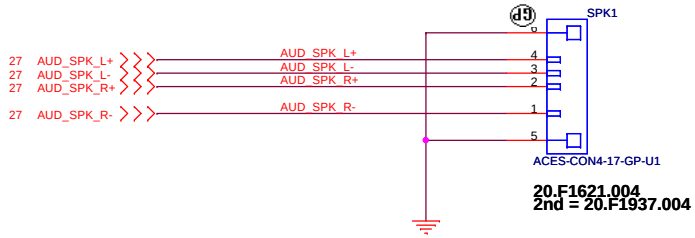
Title

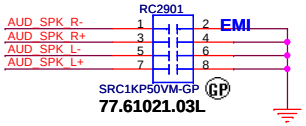
AUDIO AMP(Reserved)

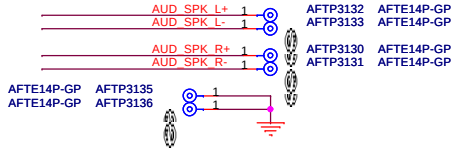
Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

Date: Wednesday, July 03, 2013 Sheet 28 of 103

Speaker Connector







<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MIC/SPEAKER/AUDIO JACK***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 29 of 103

LAN RJ45

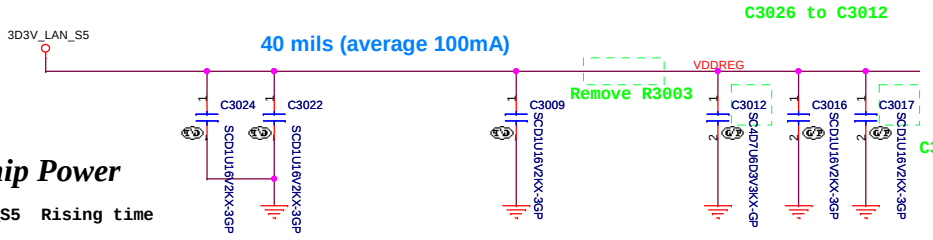
USE EFuse No ASF

DEL

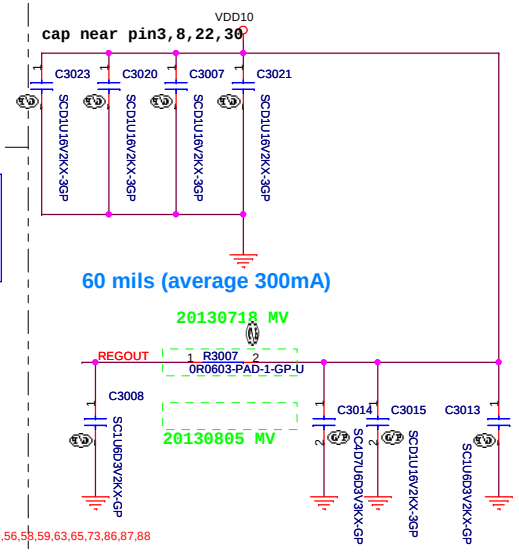
LAN CHIP-RTL8151GH

LanChip Power

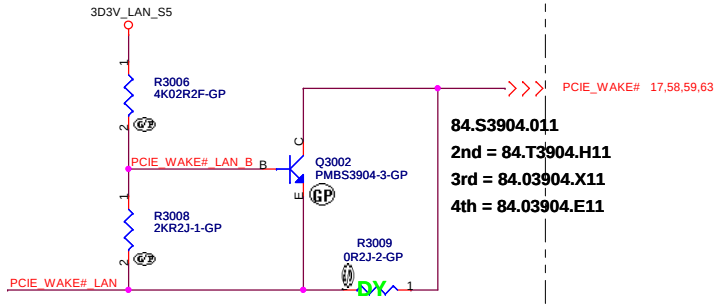
+3.3V_LAN_S5 Rising time (10%~90%)
Spec >1mS and <100mS



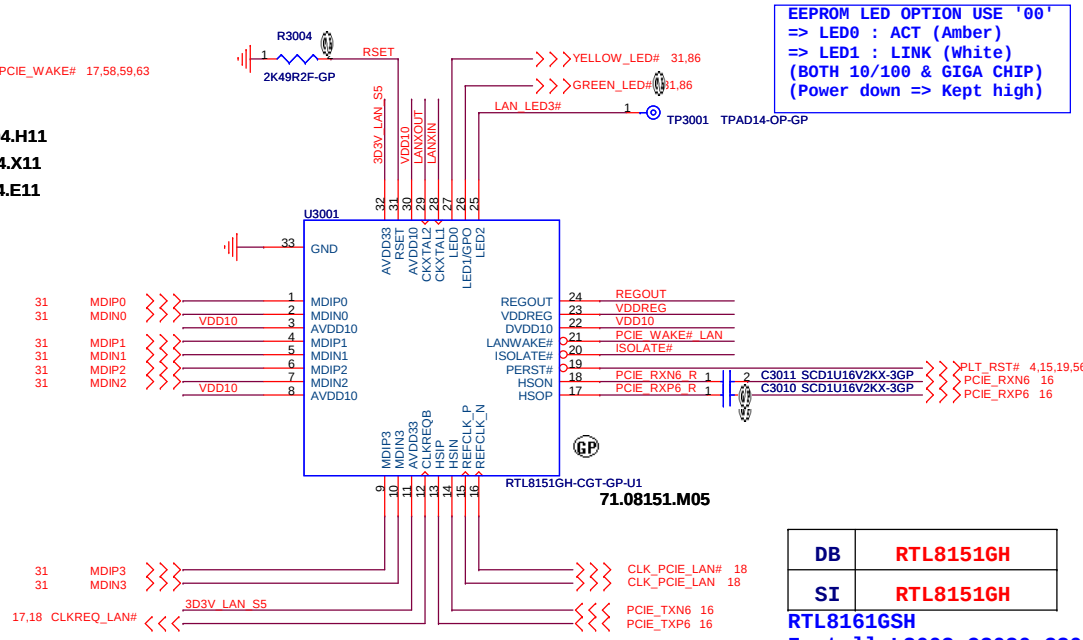
Regout power plane(1D05V)



Put 4D7U L + 4D7U cap near pin24 <200mils
(2nd = 78.22610.81L)



84.S3904.011
2nd = 84.T3904.H11
3rd = 84.03904.X11
4th = 84.03904.E11



EEPROM LED OPTION USE '00'
=> LED0 : ACT (Amber)
=> LED1 : LINK (White)
(BOTH 10/100 & GIGA CHIP)
(Power down => Kept high)

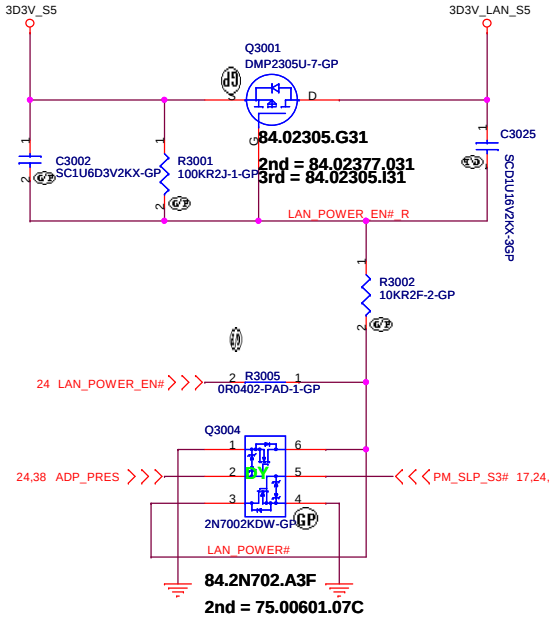
DB	RTL8151GH
SI	RTL8151GH

RTL8161GSH
Install:L3003 C3030 C3031 C3026 C3001
DY:R3007

Lan Power Inductance Spec
(1) IDC >= 600mA
(2) Tolerance < 20%
(3) RDC <= 0.8ohms(Max)
(4) Efficiency >= 80%

Regout Switch

3D3V_LAN_S5 rise time controlled between 0.5mS and 100mS.

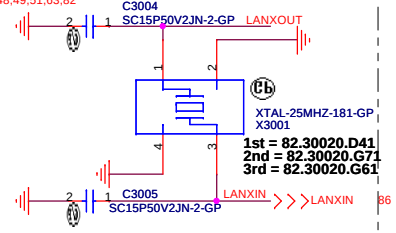


84.02305.G31
2nd = 84.02377.031
3rd = 84.02305.I31

84.2N702.A3F
2nd = 75.00601.07C

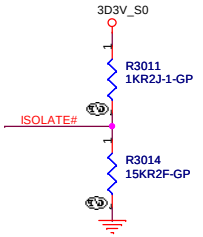
Using Efuse
Without ASF

25MHz Crystal



1st = 82.30020.D41
2nd = 82.30020.G71
3rd = 82.30020.G61

Isolate Strap Pin



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Lan Realtek 8151GH

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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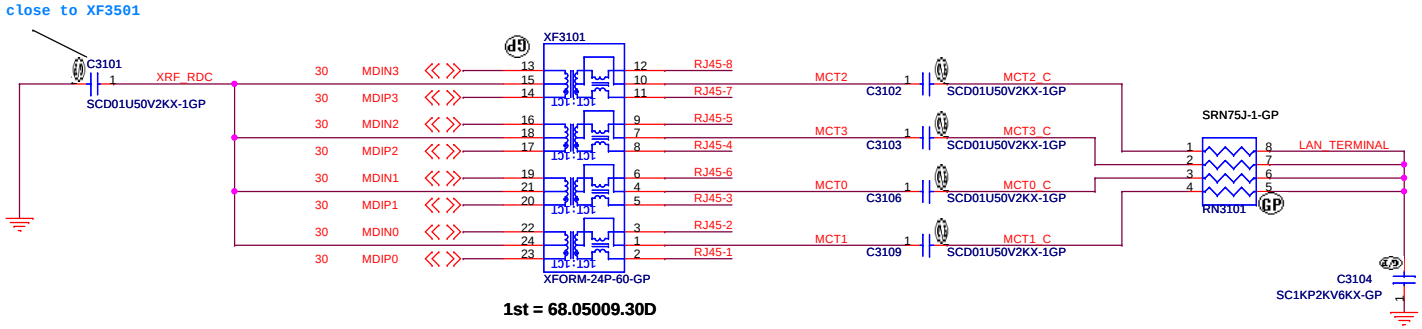
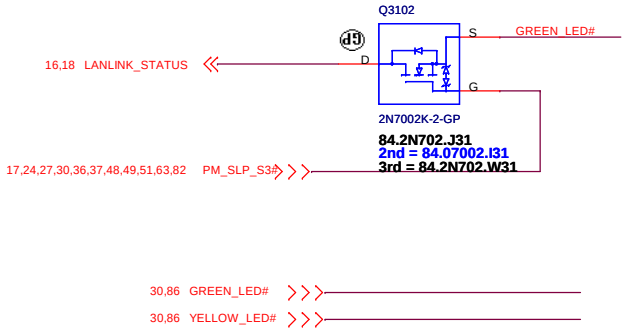
White LED for connectivity and Amber LED for activity located on RJ-45 connector



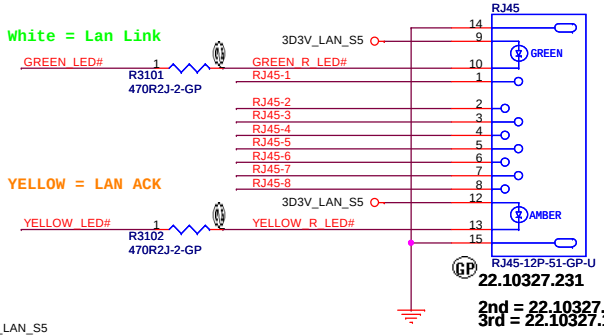
1st = 68.05009.30D
2nd = 68.89240.30D
3rd = 68.IH601.301

RJ45 Connector



84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31

wavelength : Orange 605mm need check

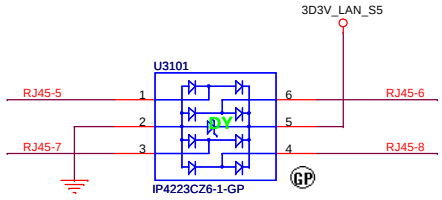


22.10327.231
2nd = 22.10327.151
3rd = 22.10327.171

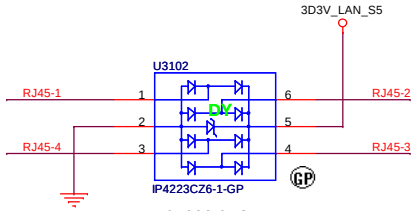
Green
10(+),9(-)

YELLOW
12(+),13(-)

(1)route on bottom as differential pairs.
(2)Tx+/Tx- are pairs. Rx+/Rx- are pairs.
(3)No vias, No 90 degree bends.
(4)pairs must be equal lengths.
(5)6mil trace width,12mil separation.
(6)36mil between pairs and any other trace.
(7)Must not cross ground moat, except RJ-45 moat.



75.04223.07C
2nd = 75.09904.07C
3rd = 75.02304.07C



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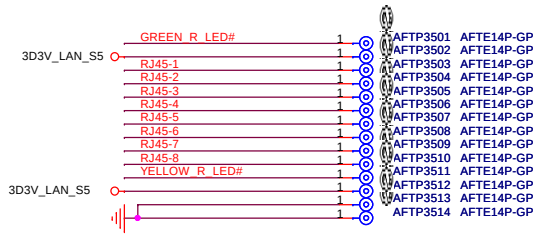
3rd = 75.02304.07C



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RJ45+Transformer

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Card Reader-JMB 709

Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

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<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

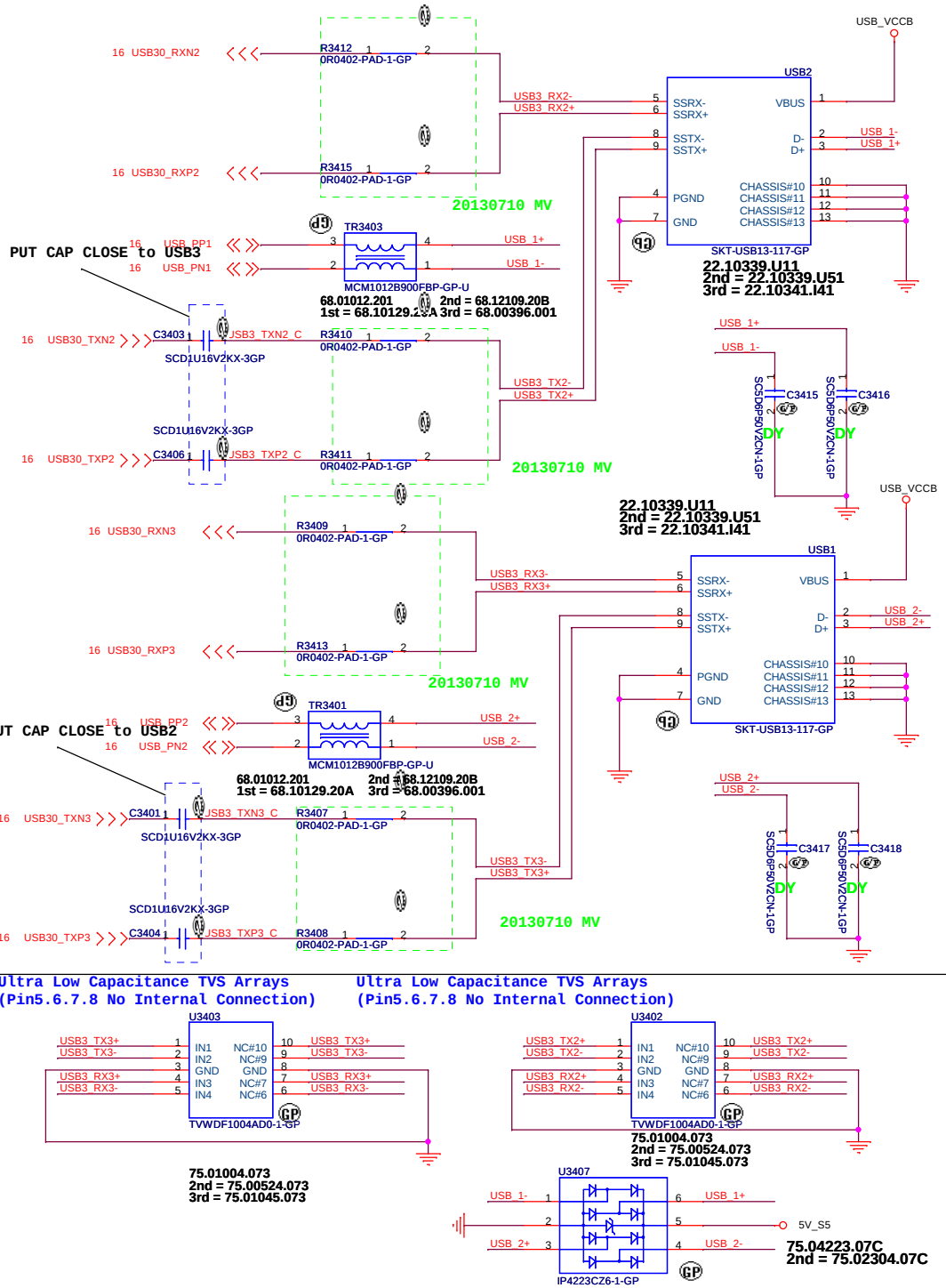
Title

CARD Reader CONN

Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

Date: Wednesday, July 03, 2013 Sheet 33 of 103

Left Side USB 3.0 Connector

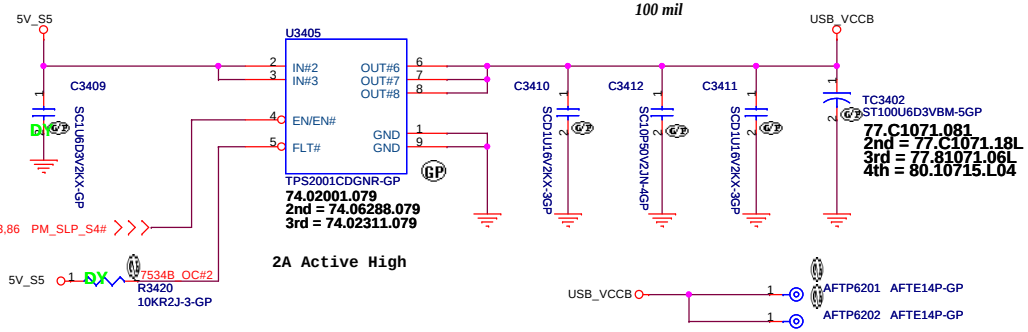


USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX-
6	StdA_SSRX+
7	GND
8	StdA_SSTX-
9	StdA_SSTX+

USB 3.0/2.0 Port Pairing

USB3.0	USB2.0
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3
Port 5	Port 4
Port 6	Port 5

USB POWER



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 2.0/ 3.0 Port

Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 34 of 103

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

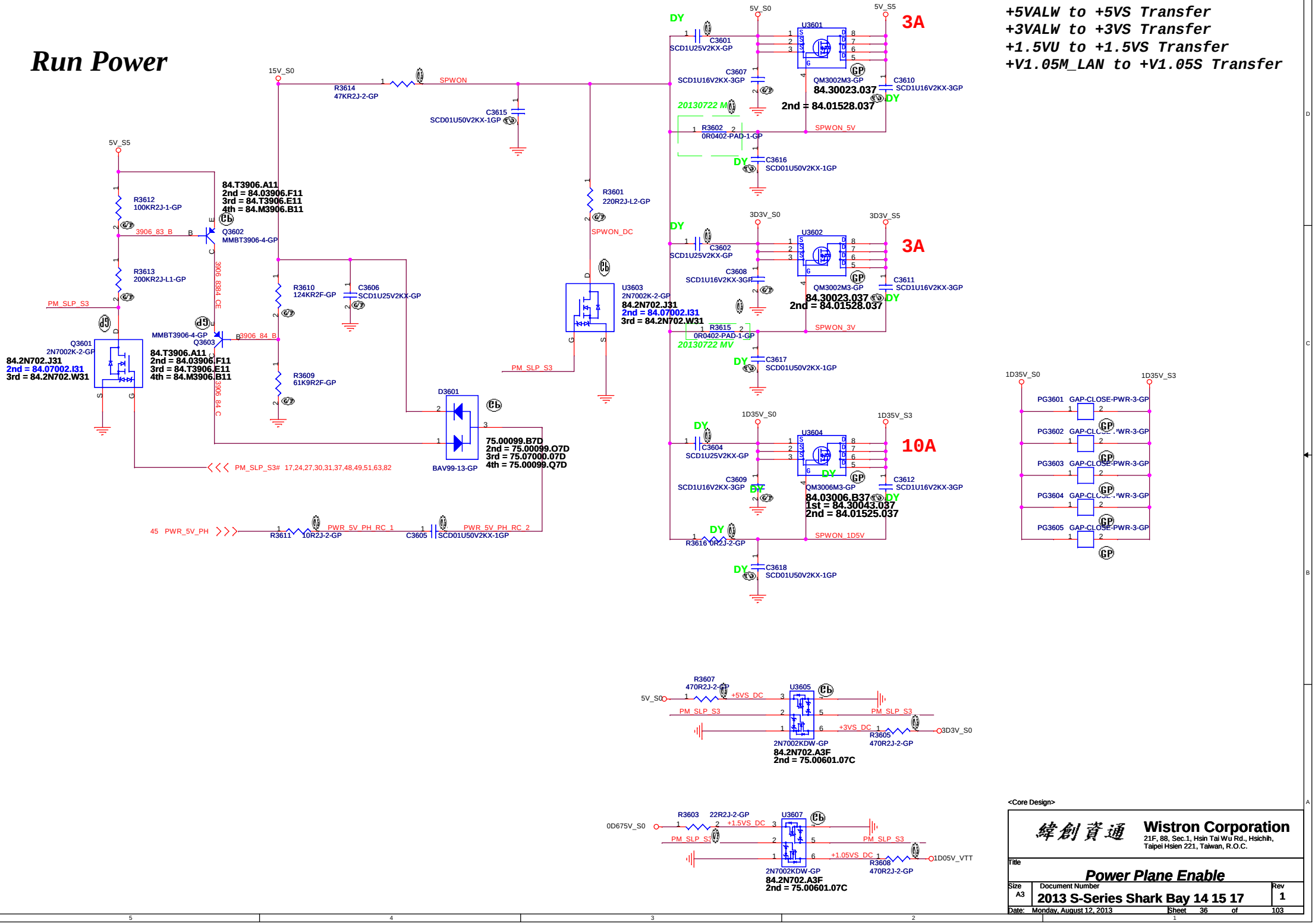
USB Charger

Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

Date: Wednesday, July 03, 2013 Sheet 35 of 103

Run Power

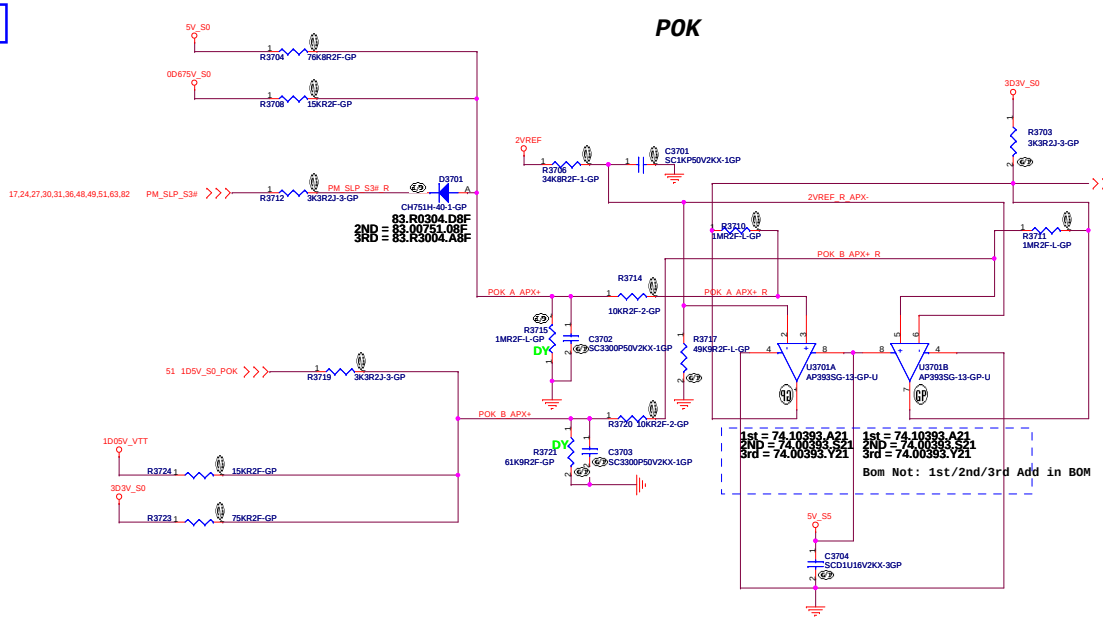
+5VALW to +5VS Transfer
+3VALW to +3VS Transfer
+1.5VU to +1.5VS Transfer
+V1.05M_LAN to +V1.05S Transfer



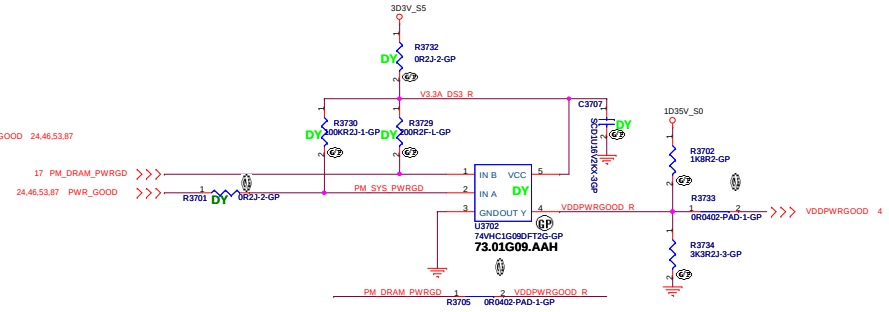
<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Power Plane Enable	
Size A3	Document Number 2013 S-Series Shark Bay 14 15 17	Rev 1
Date: Monday, August 12, 2013	Sheet 36 of 103	

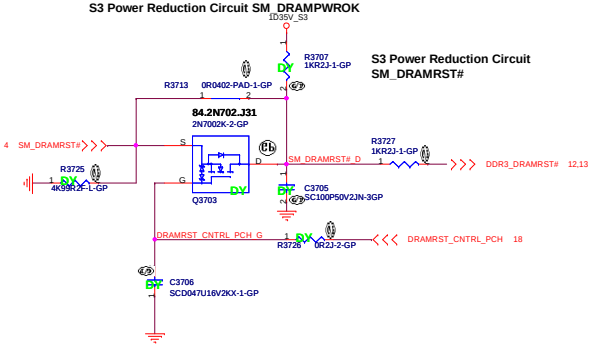
POK



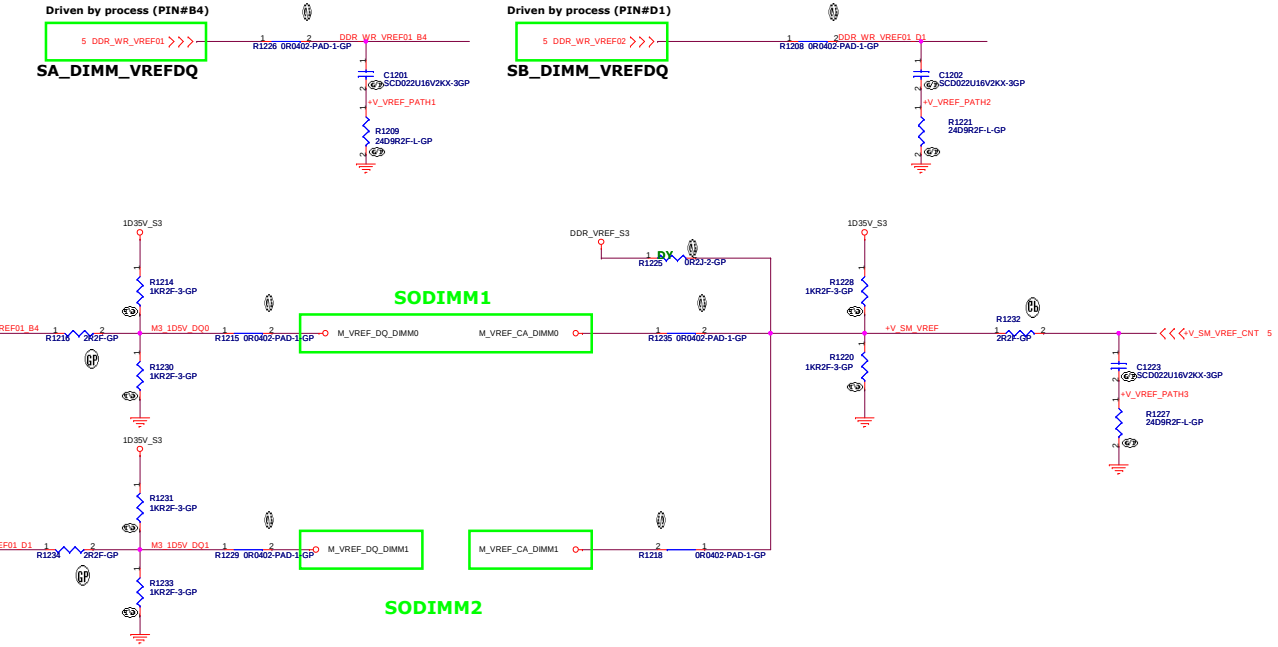
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POK

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14 15 17	1

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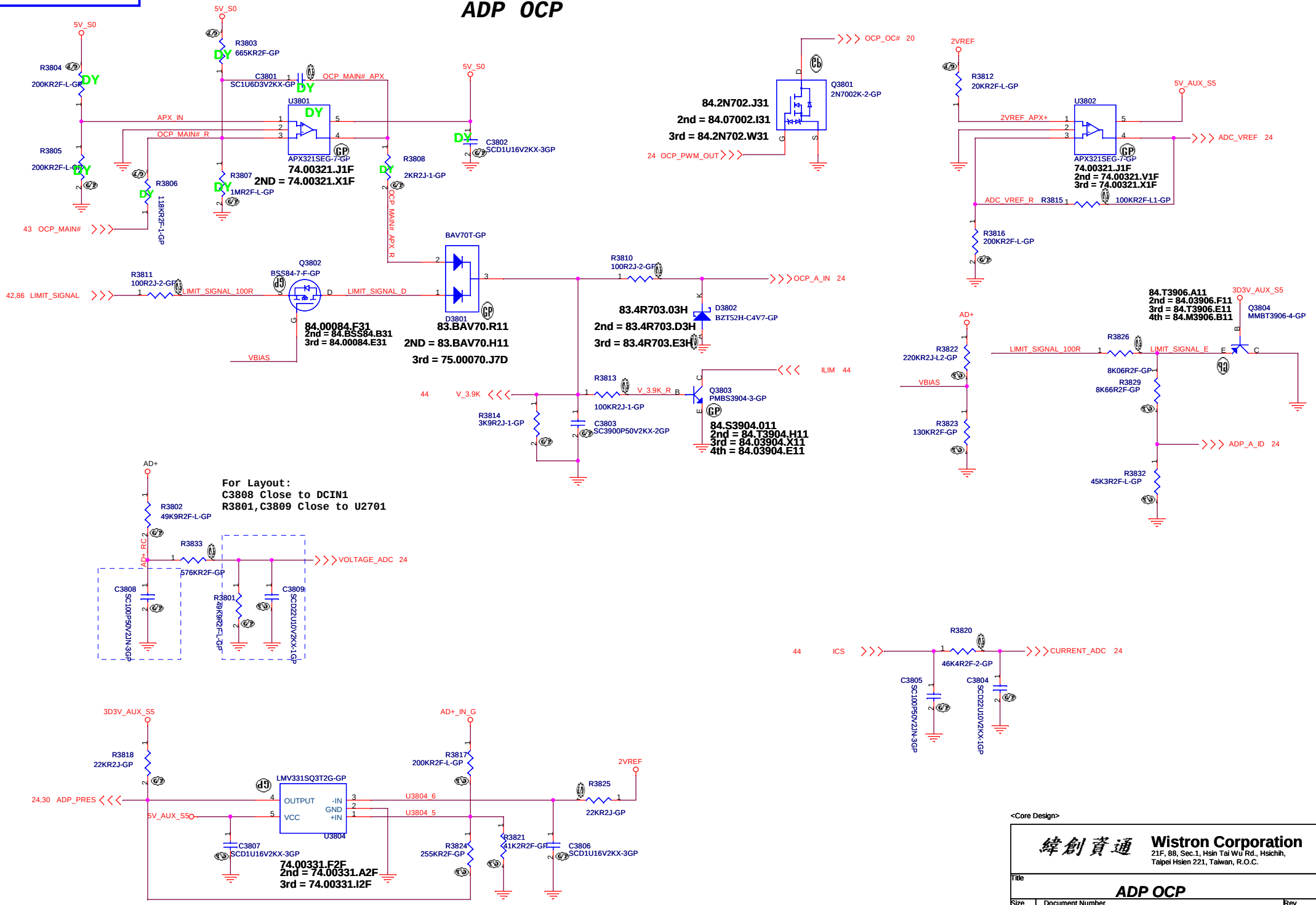
ADP OCP

ADP OCP



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADP OCP

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

1D05 M

Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

Date: Wednesday, July 03, 2013 Sheet 39 of 103

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *TPS51225_5V/3D3V*

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14 15 17	1

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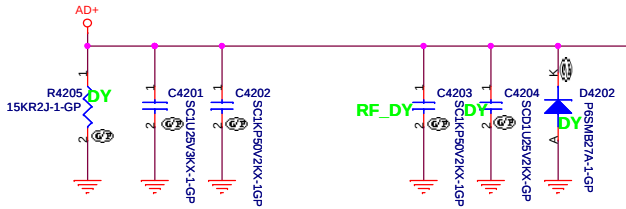
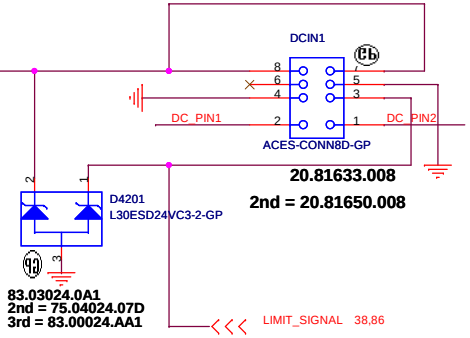
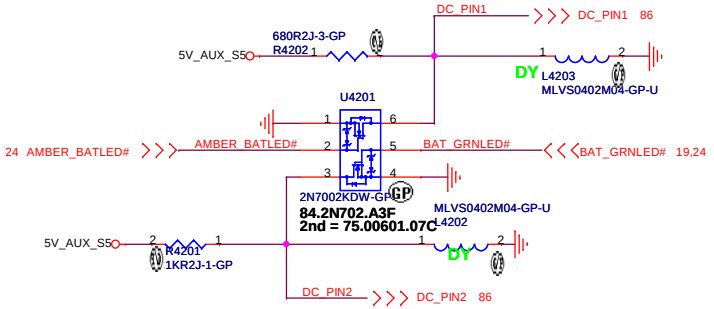
Adaptor in to generate DCBATOUT

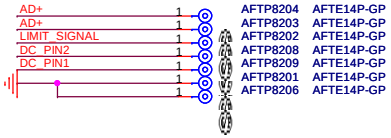


83.P6SMB.KAG

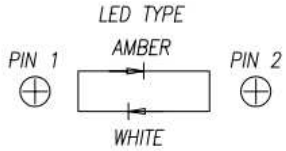
2ND = 83.P6SBM.EAG







	KBC pin 120 BAT_GRNLED#	KBC pin 113 AMBER_BATLED#
Amber	High	Low
White	Low	High
LED OFF	Low	Low



NODE		COLOR
PIN1(+)	PIN2(−)	AMBER
PIN1(−)	PIN2(+)	WHITE

<Core Design>

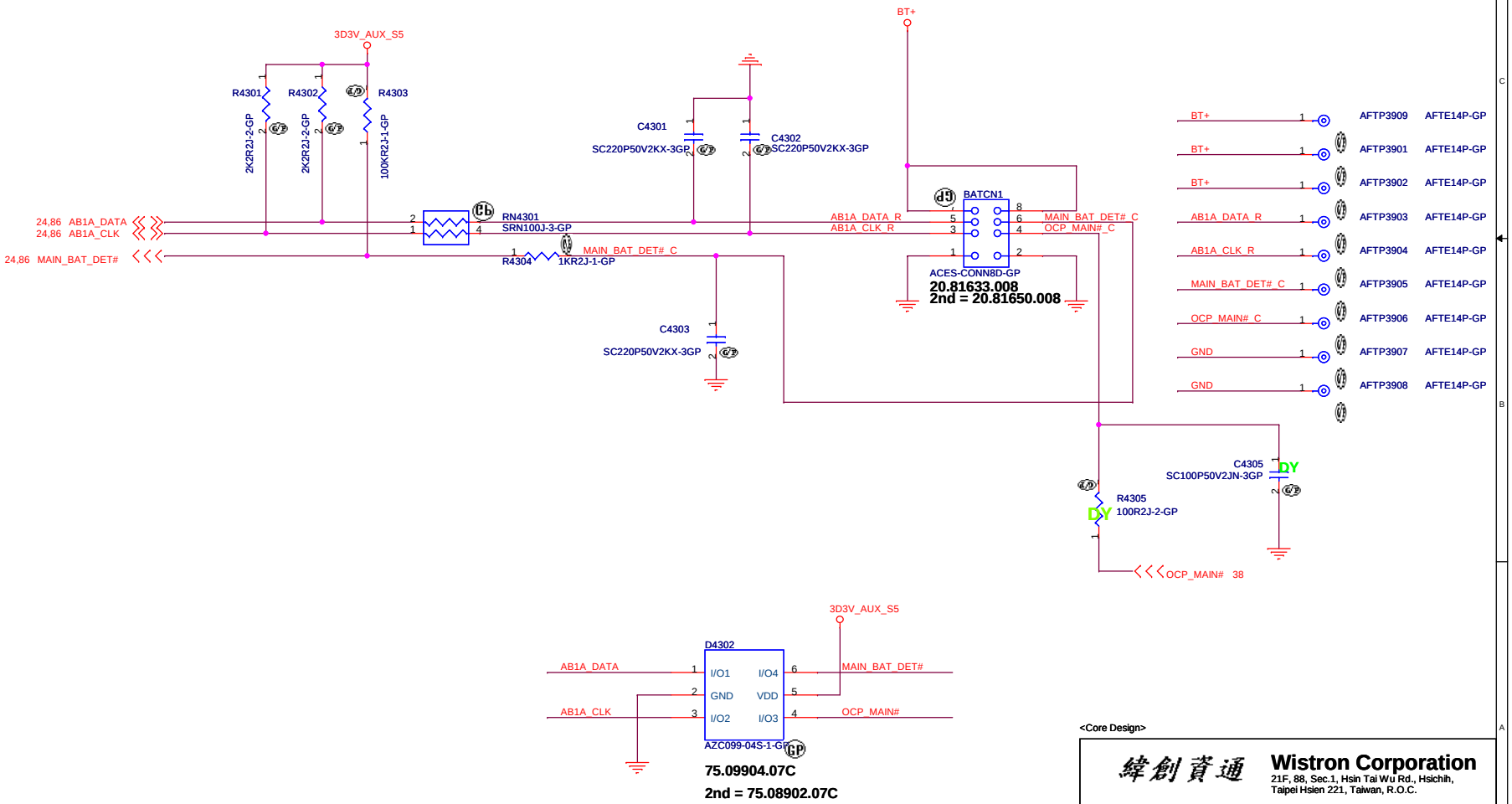
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCIN JACK**

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 42 of 103

Battery Connector



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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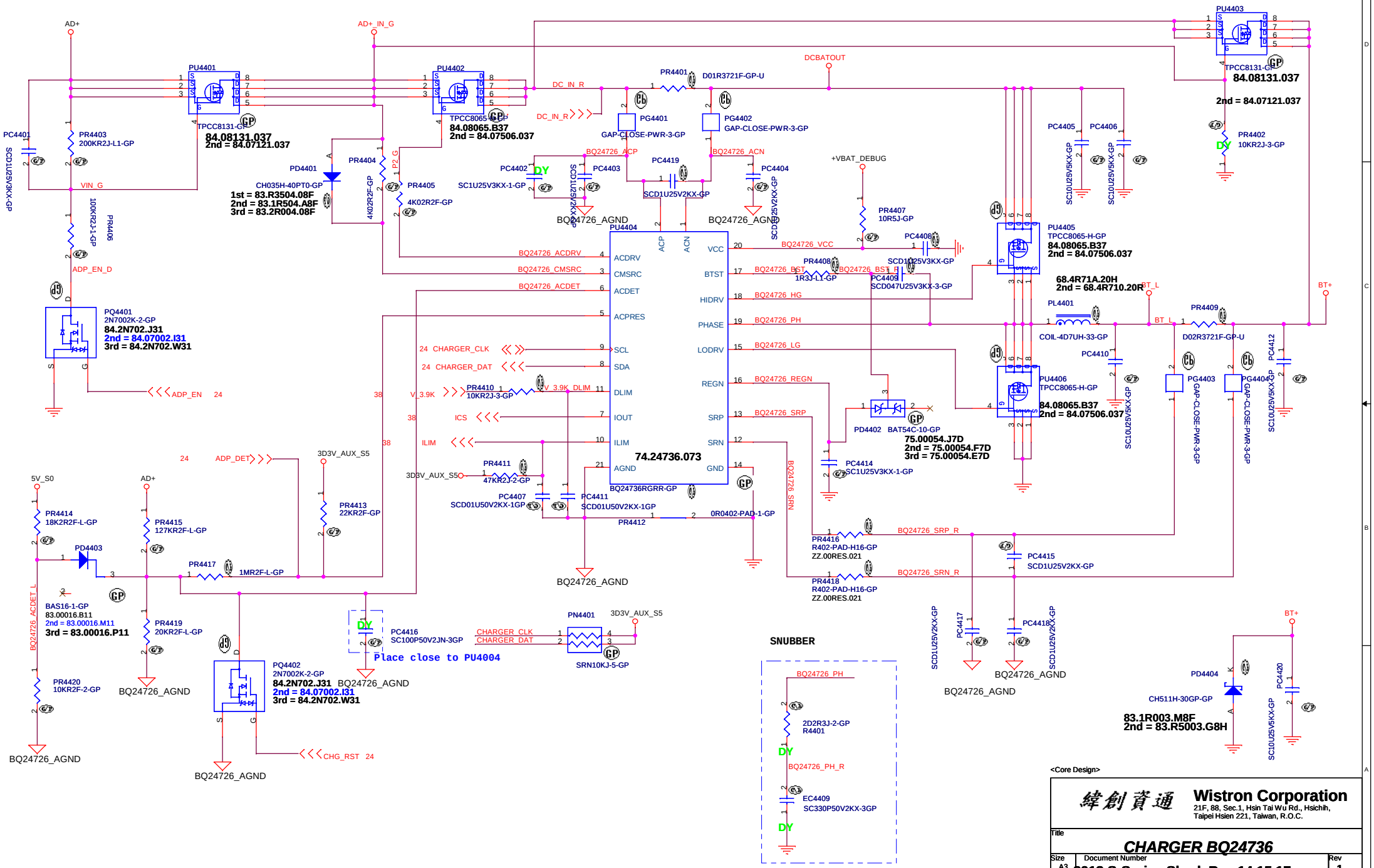
BQ24736 for CHARGER



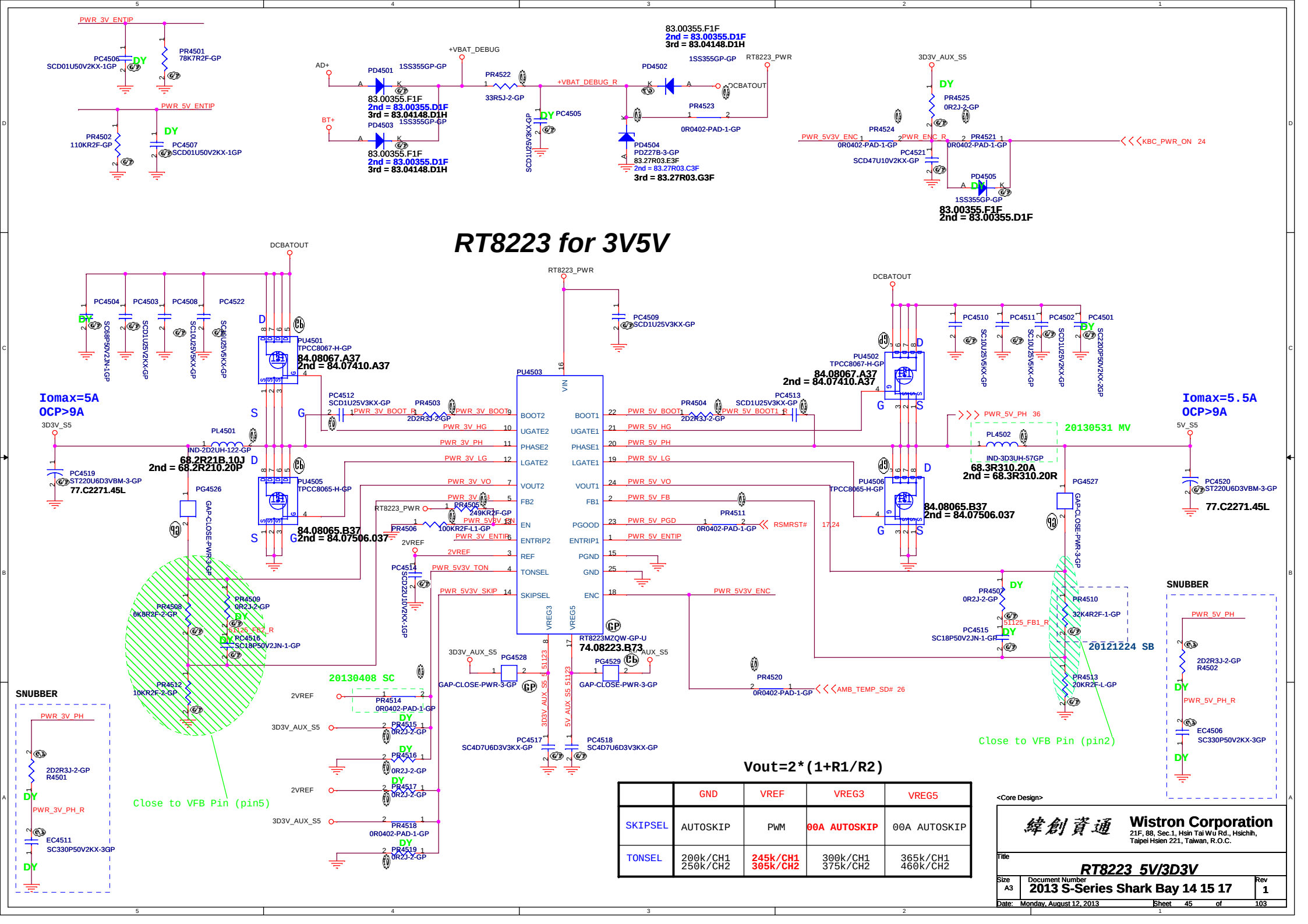
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER BQ24736**

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 44 of 103


RT8223 for 3V5V
Iomax=5A
OCP>9A
Iomax=5.5A
OCP>9A
Vout=2*(1+R1/R2)
SKIPSEL | GND | AUTOSKIP | VREF | PWM | VREG3 | 00A AUTOSKIP | VREG5 | 00A AUTOSKIP
TONSEL | GND | 200k/CH1 250k/CH2 | VREF | 245k/CH1 305k/CH2 | VREG3 | 300k/CH1 375k/CH2 | VREG5 | 365k/CH1 460k/CH2
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
SNUBBER
SNUBBER
20130408 SC
20130531 MV
20121224 SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
RT8223 5V/3D3V
2013 S-Series Shark Bay 14 15 17
Monday, August 12, 2013

37W:
PR4611 178K(64.17835.6DL)
PR4615 487K(64.48735.6DL)
PR4614 549K(64.54935.6DL)

47W:
PR4611 90.9K(64.90925.6DL)
PR4615 274K(64.27435.6DL)
PR4614 226K(64.22635.6DL)

PR4601 NTC-100K-10-GP 69.60037.031 2nd = 69.60028.011
PR4602 10KR2F-2-GP
PC4601 SC1KP50V2KX-1GP
PC4602 SC4700P50V2KX-1GP
PR4603 75R2F-2-GP DY
PR4604 39KR2F-GP PWR_VCC_SLEWA
PR4605 10KR3F-L-GP DCBATOUT PWR_VCC_VBAT
PR4611 178KR2F-GP
PR4612 39K2R2F-L-GP
PR4613 75R2F-2-GP DY
PR4614 549KR2F-GP
PR4615 487KR2F-2-GP
PR4616 150KR2F-L-GP
PR4617 150KR2F-L-GP
PR4618 150KR2F-L-GP
PWR_VCC_VREF
PWR_VCC_B-RAMP
PWR_VCC_F-Imax
PWR_VCC_O-USR
PWR_VCC_THERM
PWR_VCC_IMON
PWR_VCC_OCP-1

PU4601 TPS51631RSMR-1-GP 74.51631.A73
VBAT SLEWA THERM IMON OCP-I B-RAMP F-IMAX O-USR
CSP1 CSN1 CSN2 CSP2 CSP3 CSN3 GFB VFB
VR_ON SKIP# PWM1 PWM2 PWM3 PGOOD VDD VDIO
DROOP COMP VREF V5A GND VR_HOT# VCLK ALERT# GND

PC4610 SC1U6D3V2KX-GP
PR4624 61K9R2F-GP 20130802 MV
PWR_GOOD_C
PWR_GOOD 24,37,53,87
PWR_VCC_SKIP# 47
PWR_VCC_PWM1 47
PWR_VCC_PWM2 47
PWR_VCC_PWM3
PR4620 75R2F-2-GP DY
PM_PWROK 6,17
PWR_VCC_VDD
PR4621 10R3F-GP 3D3V_S5
PC4606 SC1U25V3KX-1GP

3D3V_S5
PR4627 0R0402-PAD-1-GP
PR4628 0R0402-PAD-1-GP
PR4610 0R0402-PAD-1-GP
PR4609 0R0402-PAD-1-GP
PWR_VCC_CSP3_R
PWR_VCC_CSN3_R
47 PWR_VCC_CSP1
47 PWR_VCC_CSN1
47 PWR_VCC_CSN2
47 PWR_VCC_CSP2
7,9 VSS_SENSE
7 VCC_SENSE
PWR_VCC_GFB
PWR_VCC_VFB

PR4619 2KR2F-3-GP 3D3V_S0 PM_PWROK 6,17

PWR_VCC_DROOP
PC4603 SC100P50V2JN-3GP
PR4606 10KR2F-2-GP
PWR_VCC_COMP
PR4607 2K94R2F-GP PWR_VCC_VREF
PR4625 10KR2F-2-GP
PC4609 SC330P50V2KX-3GP
PWR_VCC_DROOP_R
PC4604 SCD33U6D3V2KX-1GP
PWR_VCC_V5A

H_CPU_SVIDDAT 7
VR_SVID_ALERT# 7
H_CPU_SVIDCLK 7
H_PROCHOT# 4

PR4608 10R3F-GP 5V_S5
PC4605 SC1U25V3KX-1GP
PC4608 SC47P50V2JN-3GP DY

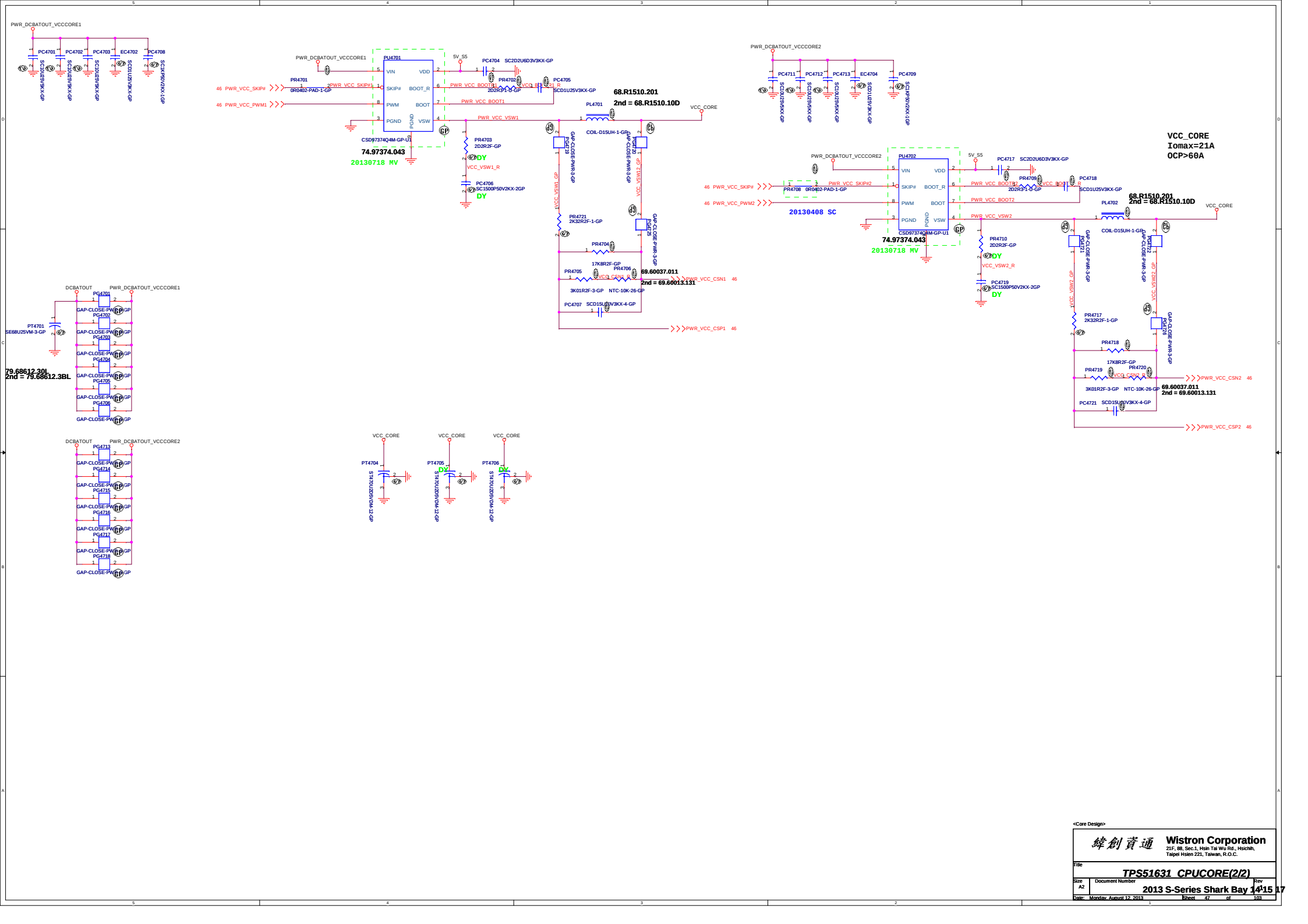
VCCIO_OUT
PC4607 SCD1U16V2KX-3GP
PR4622 130R2F-1-GP H_CPU_SVIDDAT
PR4623 54D9R2F-L1-GP H_CPU_SVIDCLK

PR4622 close to PU4601

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51631_CPUCORE(1/2)
Size: A3 Document Number: 2013 S-Series Shark Bay 14 15 17 Rev: 1
Date: Monday, August 12, 2013 Sheet 46 of 103


PWR_DCBATOUT_VCCCORE1
PC4701
PC4702
PC4703
EC4702
PC4708
PU4701
VIN
VDD
SKIP#
BOOT_R
PWM
BOOT
PGND
VSW
CSD97374Q4M-GP-U1
PR4701
0R0402-PAD-1-GP
PWR_VCC_SKIP#1
PWR_VCC_PWM1
PWR_VCC_BOOT1
PWR_VCC_VSW1
5V_S5
PC4704
SC2D2U6D3V3KX-GP
PR4702
2D2R3F1-0-GP
PC4705
SCD1U25V3KX-GP
68.R1510.201
2nd = 68.R1510.10D
PL4701
COIL-D15UH-1-GP
VCC_CORE
74.97374.043
20130718 MV
PR4703
2D2R2F-GP
DY
PC4706
SC1500P50V2KX-2GP
GAP-CLOSE-PWR-3-GP
PR4721
2K32R2F-1-GP
PR4704
17K8R2F-GP
PR4705
3K01R2F-3-GP
NTC-10K-26-GP
PR4706
69.60037.011
2nd = 69.60013.131
PC4707
SCD15U25V3KX-4-GP
PWR_VCC_CSN1
PWR_VCC_CSP1
PWR_DCBATOUT_VCCCORE2
PC4711
PC4712
PC4713
EC4704
PC4709
PU4702
PR4708
0R0402-PAD-1-GP
PWR_VCC_SKIP#2
PWR_VCC_PWM2
PWR_VCC_BOOT2
PWR_VCC_VSW2
PC4717
SC2D2U6D3V3KX-GP
PR4709
2D2R3F1-0-GP
PC4718
SCD1U25V3KX-GP
68.R1510.201
2nd = 68.R1510.10D
PL4702
COIL-D15UH-1-GP
VCC_CORE
74.97374.043
20130718 MV
20130408 SC
PR4710
2D2R2F-GP
PC4719
SC1500P50V2KX-2GP
PR4717
2K32R2F-1-GP
PR4718
17K8R2F-GP
PR4719
3K01R2F-3-GP
NTC-10K-26-GP
PR4720
69.60037.011
2nd = 69.60013.131
PC4721
SCD15U25V3KX-4-GP
PWR_VCC_CSN2
PWR_VCC_CSP2
VCC_CORE
Iomax=21A
OCP>60A
DCBATOUT
PWR_DCBATOUT_VCCCORE1
PT4701
SE68U25VM-3-GP
79.68612.30L
2nd = 79.68612.3BL
PG4701
PG4702
PG4703
PG4704
PG4705
PG4706
GAP-CLOSE-PWR-GP
DCBATOUT
PWR_DCBATOUT_VCCCORE2
PG4713
PG4714
PG4715
PG4716
PG4717
PG4718
VCC_CORE
PT4704
PT4705
PT4706
DY
ST470U2D5VDM-12-GP
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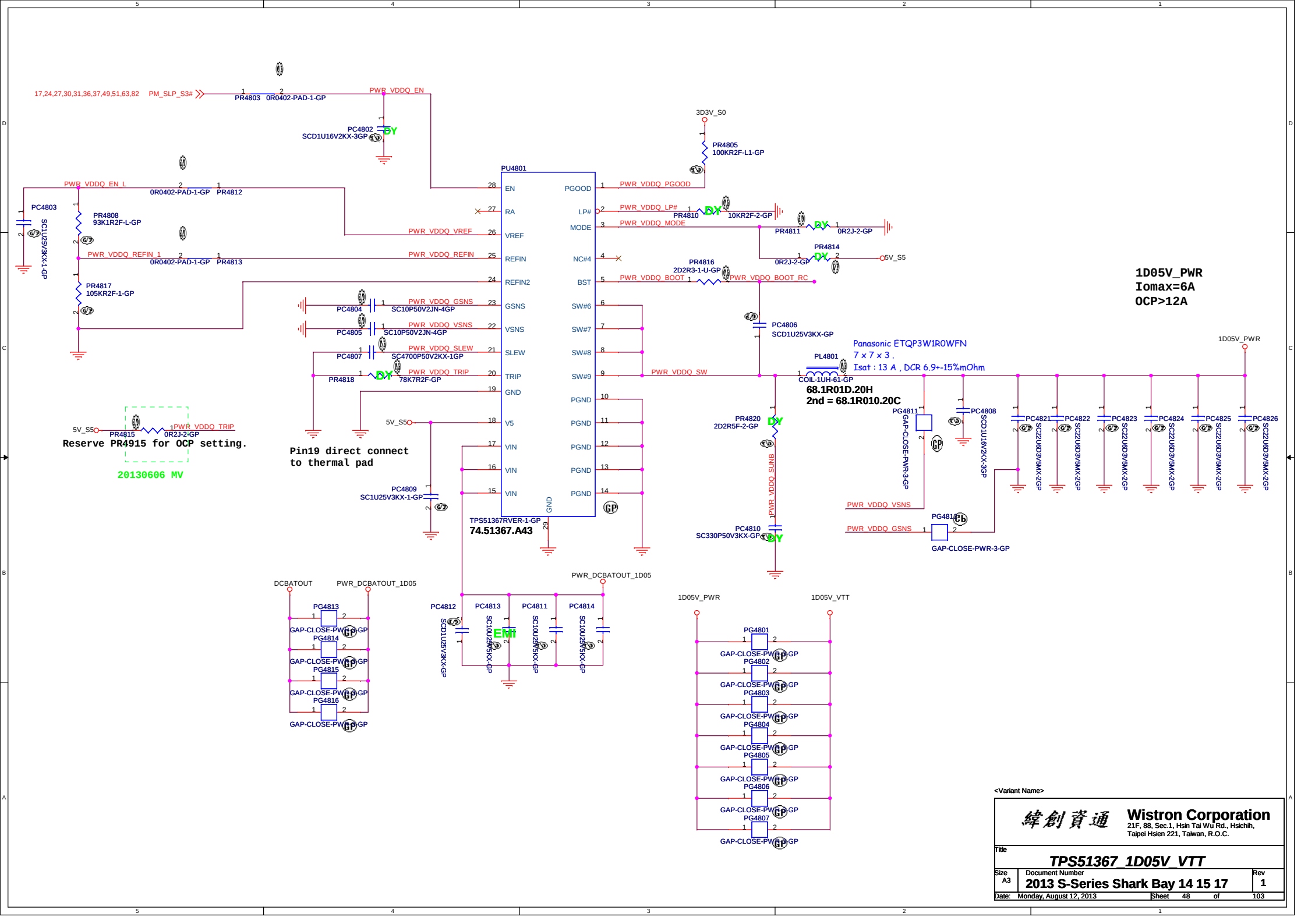
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51631_CPUCORE(2/2)
Size
A2
Document Number
2013 S-Series Shark Bay 14"15"17
Rev
Date: Monday, August 12, 2013
Sheet 47 of 103



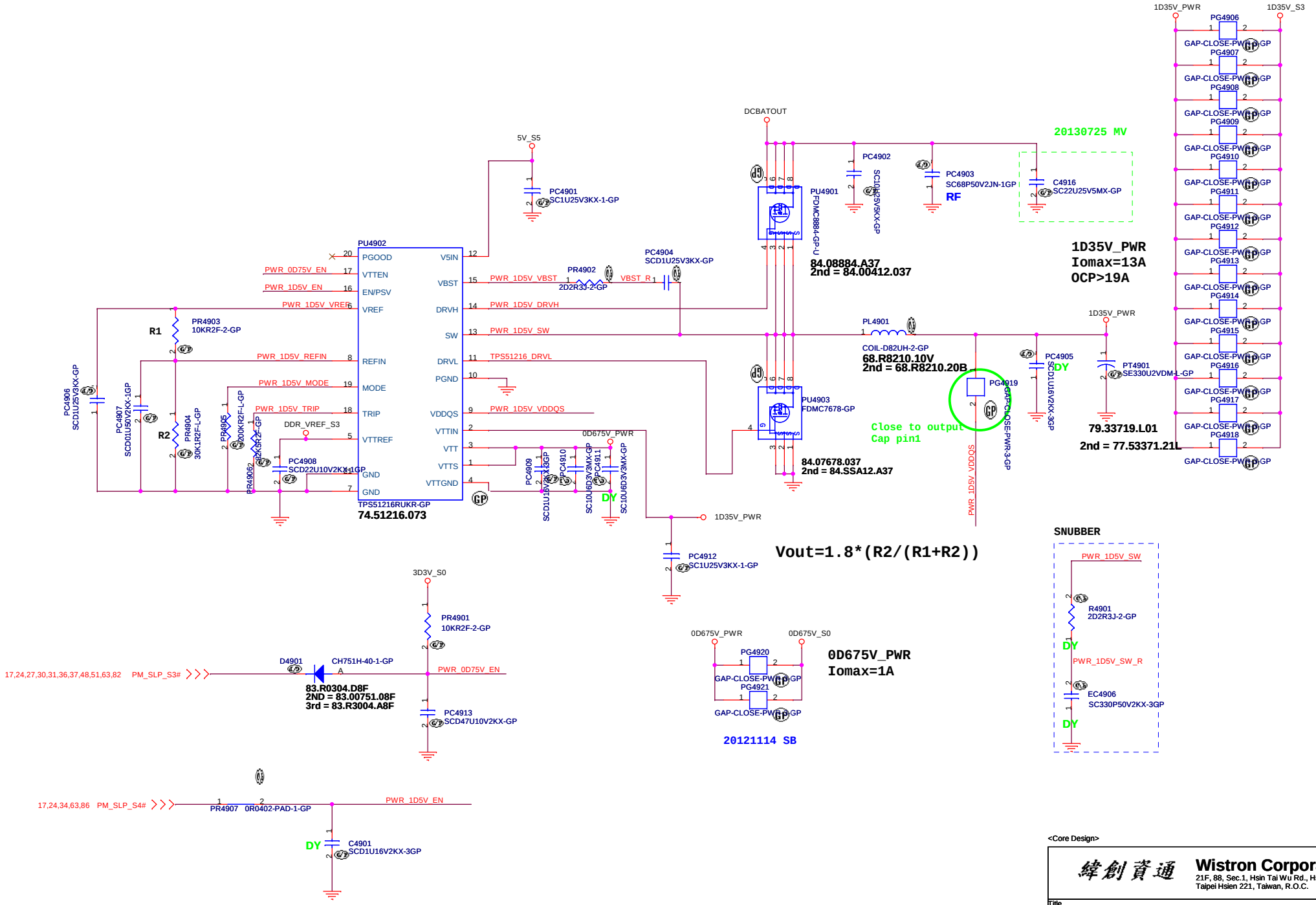
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51367_1D05V_VTT***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 48 of 103


PU4902
TPS51216RUKR-GP
74.51216.073
PGOOD
VTTEN
EN/PSV
VREF
REFIN
MODE
TRIP
VTTREF
GND
GND
V5IN
VBST
DRVH
SW
DRVL
PGND
VDDQS
VTTIN
VTT
VTTS
VTTGND
PWR_0D75V_EN
PWR_1D5V_EN
PWR_1D5V_VREF
PWR_1D5V_REFIN
PWR_1D5V_MODE
PWR_1D5V_TRIP
PWR_1D5V_VBST
PWR_1D5V_DRVH
PWR_1D5V_SW
TPS51216_DRVL
PWR_1D5V_VDDQS
VBST_R
DDR_VREF_S3
5V_S5
DCBATOUT
0D675V_PWR
1D35V_PWR
3D3V_S0
PU4901
FDMC8884-GP-U
84.08884.A37
2nd = 84.00412.037
PU4903
FDMC7678-GP
84.07678.037
2nd = 84.SSA12.A37
PL4901
COIL-D82UH-2-GP
68.R8210.10V
2nd = 68.R8210.20B
79.33719.L01
2nd = 77.53371.21L
Close to output Cap pin1
20130725 MV
1D35V_PWR
Iomax=13A
OCP>19A
RF
DY
Vout=1.8*(R2/(R1+R2))
0D675V_PWR
Iomax=1A
20121114 SB
SNUBBER
PM_SLP_S3#
PM_SLP_S4#
17,24,27,30,31,36,37,48,51,63,82
17,24,34,63,86
D4901
CH751H-40-1-GP
83.R0304.D8F
2ND = 83.00751.08F
3rd = 83.R3004.A8F
PR4901 10KR2F-2-GP
PR4907 0R0402-PAD-1-GP
R4901 2D2R3J-2-GP
EC4906 SC330P50V2KX-3GP
C4901 SCD1U16V2KX-3GP
PC4913 SCD47U10V2KX-GP
PC4908 SCD22U10V2KX-1GP
PC4912 SC1U25V3KX-1-GP
PC4901 SC1U25V3KX-1-GP
PC4902 SC10U25V5KX-GP
PC4903 SC68P50V2JN-1GP
C4916 SC22U25V5MX-GP
PC4904 SCD1U25V3KX-GP
PC4905 SCD1U16V2KX-3GP
PT4901 SE330U2VDM-L-GP
PG4919 GAP-CLOSE-PWR-3-GP
PG4920 GAP-CLOSE-PWR-GP
PG4921 GAP-CLOSE-PWR-GP
PG4906 GAP-CLOSE-PWR-GP
PG4907 GAP-CLOSE-PWR-GP
PG4908 GAP-CLOSE-PWR-GP
PG4909 GAP-CLOSE-PWR-GP
PG4910 GAP-CLOSE-PWR-GP
PG4911 GAP-CLOSE-PWR-GP
PG4912 GAP-CLOSE-PWR-GP
PG4913 GAP-CLOSE-PWR-GP
PG4914 GAP-CLOSE-PWR-GP
PG4915 GAP-CLOSE-PWR-GP
PG4916 GAP-CLOSE-PWR-GP
PG4917 GAP-CLOSE-PWR-GP
PG4918 GAP-CLOSE-PWR-GP
R1
R2
PR4903 10KR2F-2-GP
PR4904 30K1R2F-LGP
PR4905 200KR2F-LGP
PR4906 20KR2F-GP
PC4906 SCD1U25V3KX-GP
PC4907 SCD01U50V2KX-1GP
PC4909 SCD1U16V2KX-3GP
PC4910 SC10U6D3V3MX-GP
PC4911 SC10U6D3V3MX-GP
PR4902 2D2R3J-2-GP
1D35V_S3
PWR_1D5V_SW_R
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51216 1D35V & 0D675V
Size A3
Document Number
2013 S-Series Shark Bay 14 15 17
Rev 1
Date: Monday, August 12, 2013
Sheet 49 of 103

(Blanking)

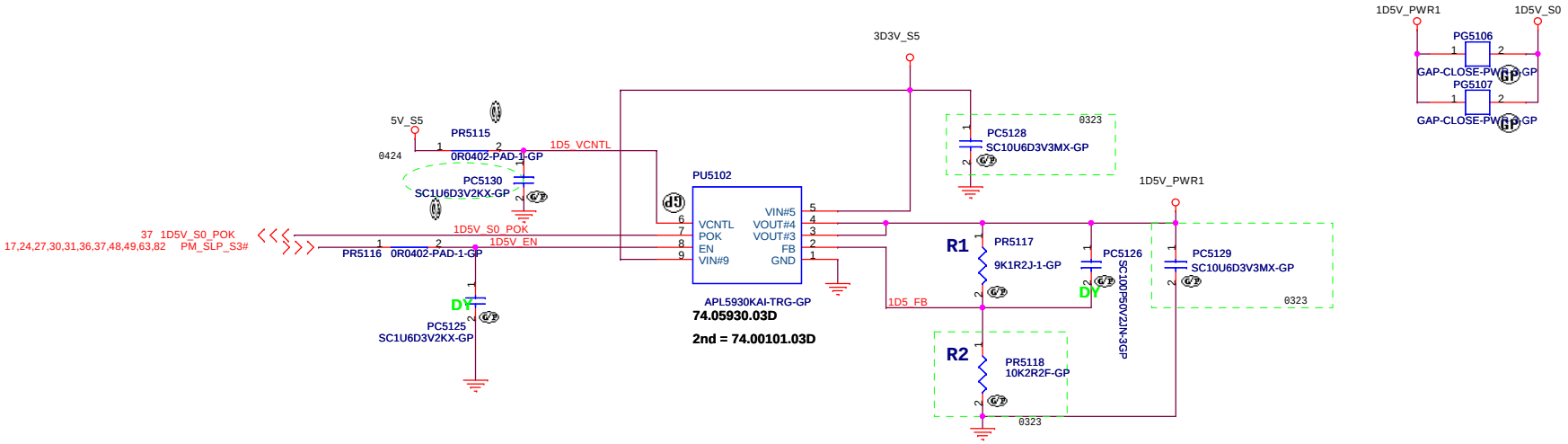
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1.1

Date: Wednesday, July 03, 2013 Sheet 50 of 103



<Core Design>

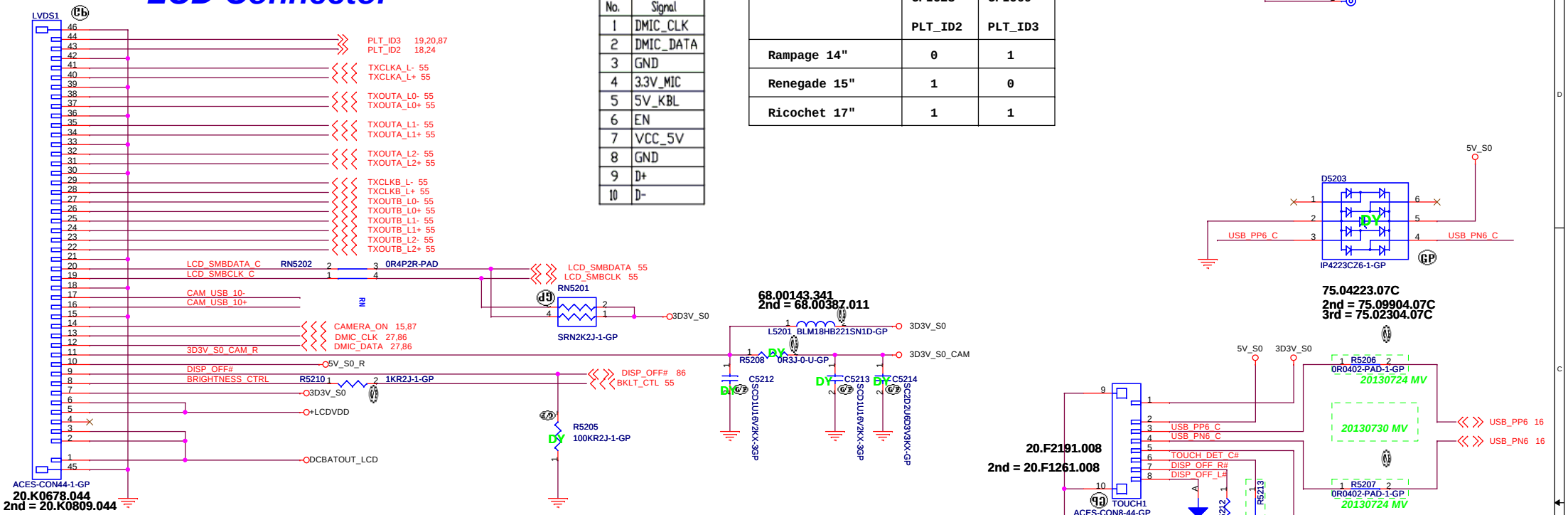
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***APL5930_1D5V_S0***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 51 of 103

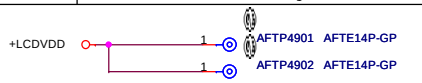
LCD Connector



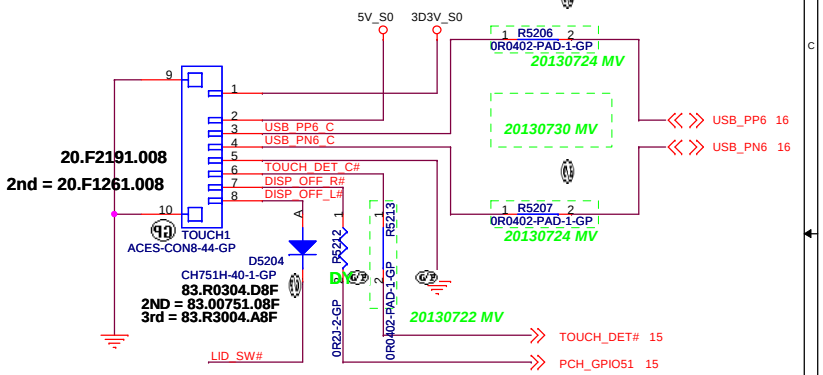
Camera Pin Define

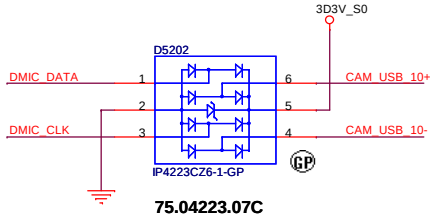
No.	Signal
1	DMIC_CLK
2	DMIC_DATA
3	GND
4	3.3V_MIC
5	5V_KBL
6	EN
7	VCC_5V
8	GND
9	D+
10	D-

	GPIO23 PLT_ID2	GPIO69 PLT_ID3
Rampage 14"	0	1
Renegade 15"	1	0
Ricochet 17"	1	1

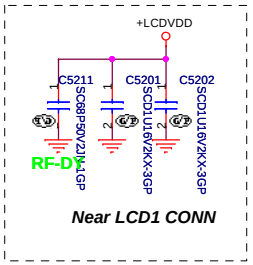


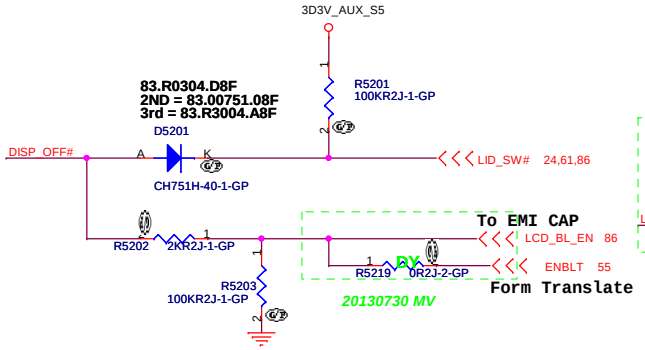
75.04223.07C
2nd = 75.09904.07C
3rd = 75.02304.07C

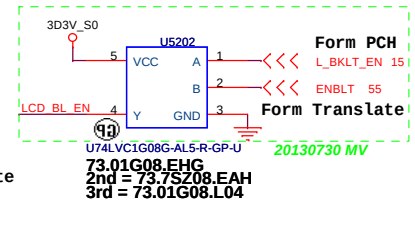


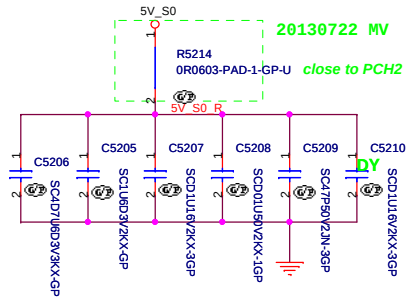


75.04223.07C
2nd = 75.02304.07C

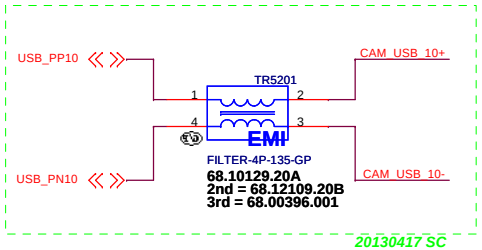




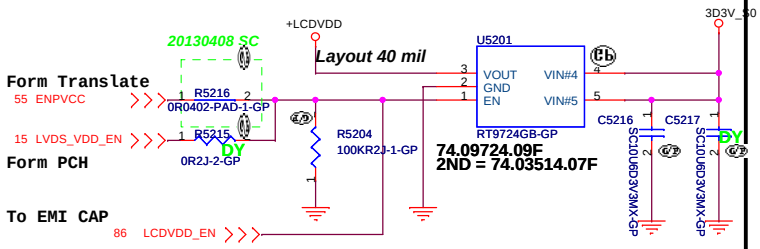




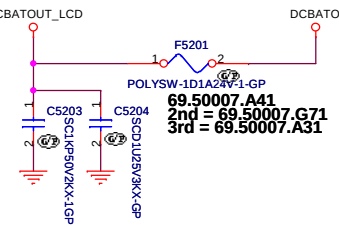
CAMERA



LCD POWER CIRCUIT



LED BACKLIGHT CONVERTER POWER



<Variant Name>

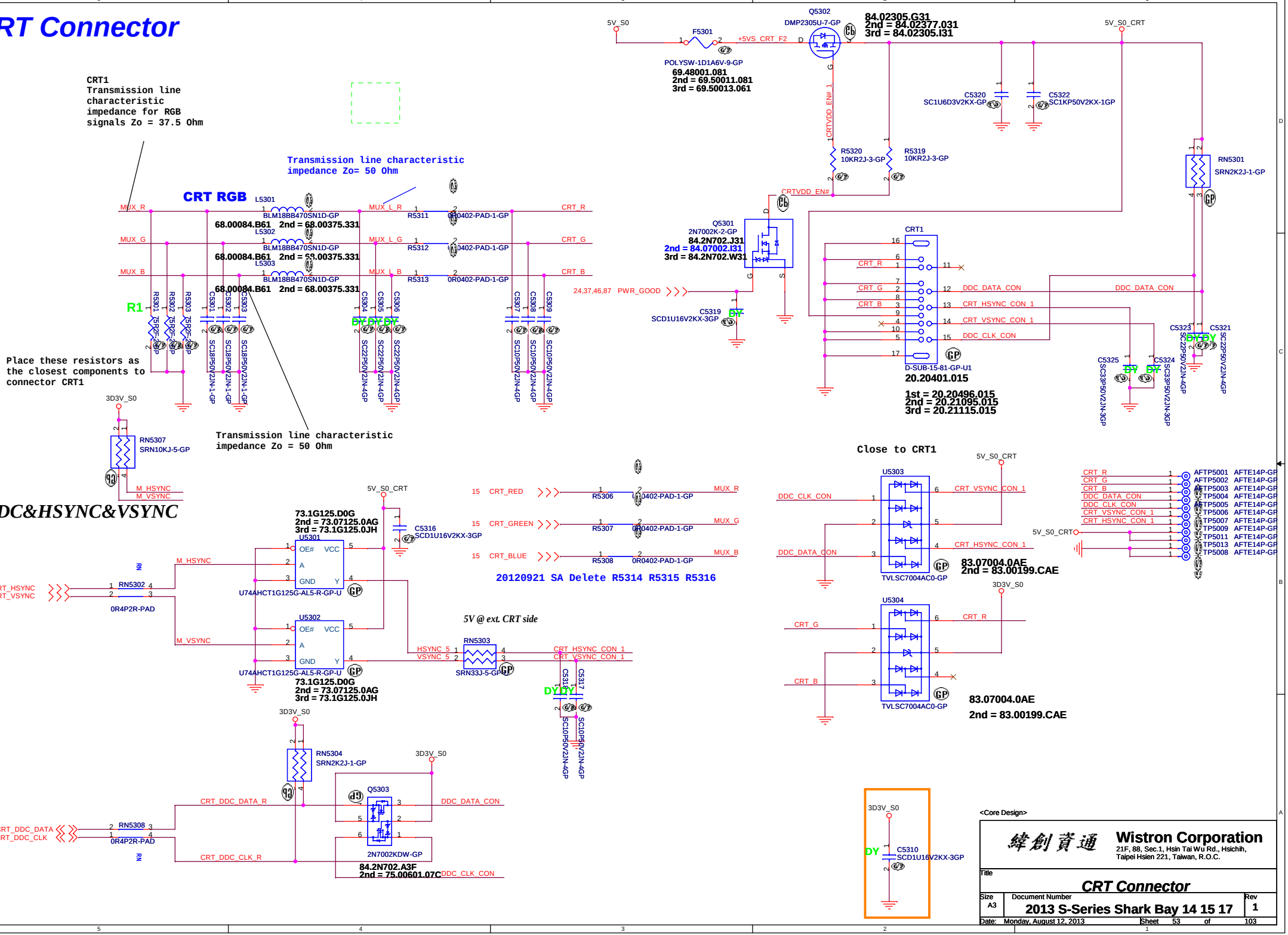
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 52 of 103

CRT Connector



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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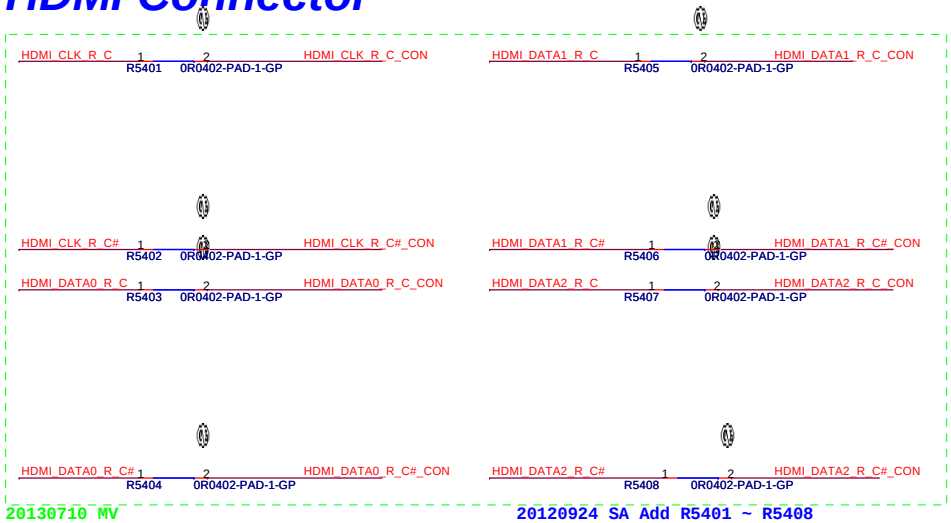
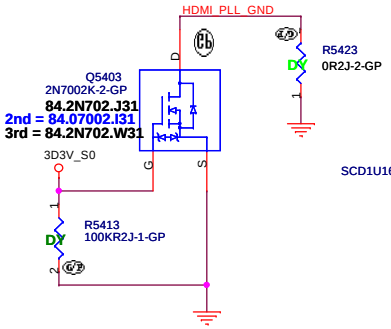
HDMI Connector

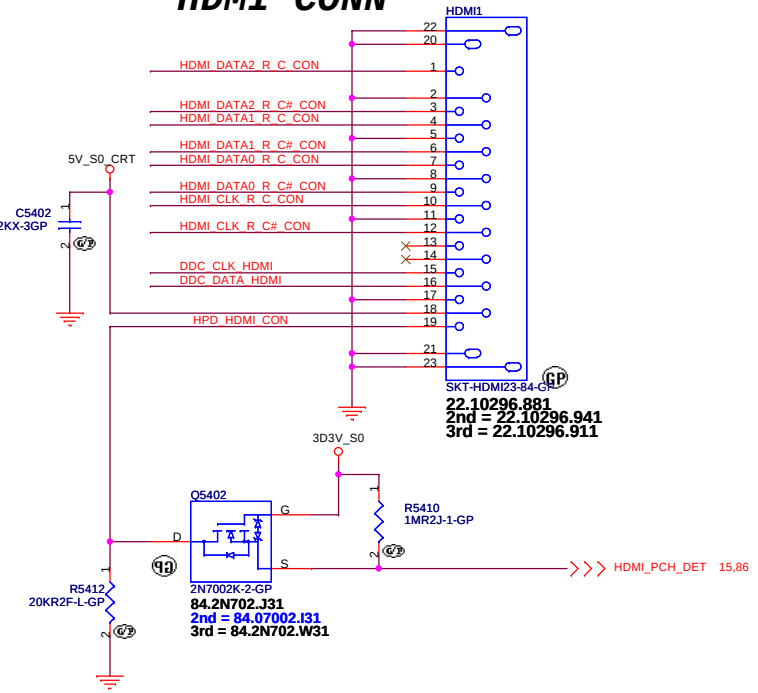


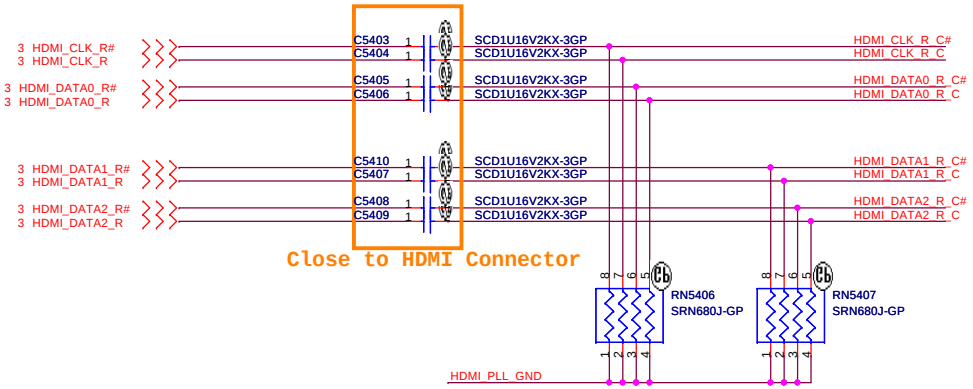
20130710 MV

20120924 SA Add R5401 ~ R5408

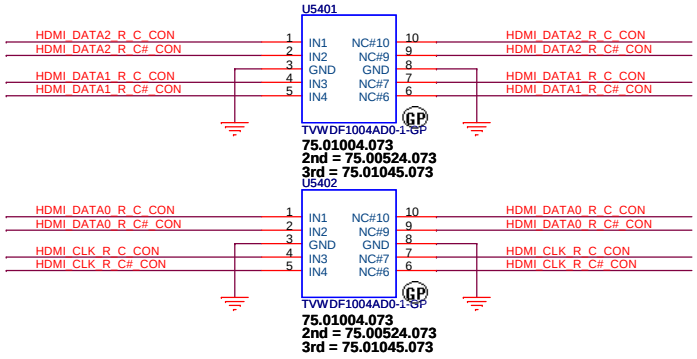


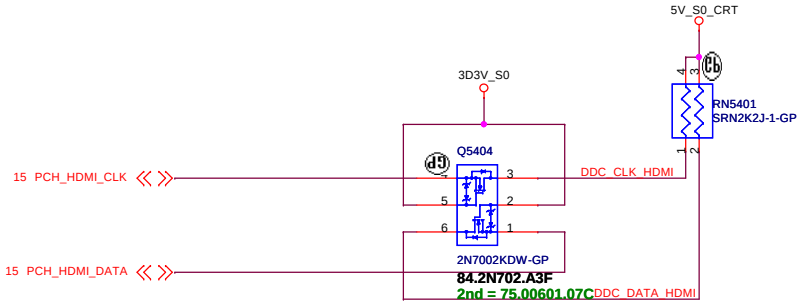
HDMI CONN





Close to HDMI1





Routing Guidelines:
CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

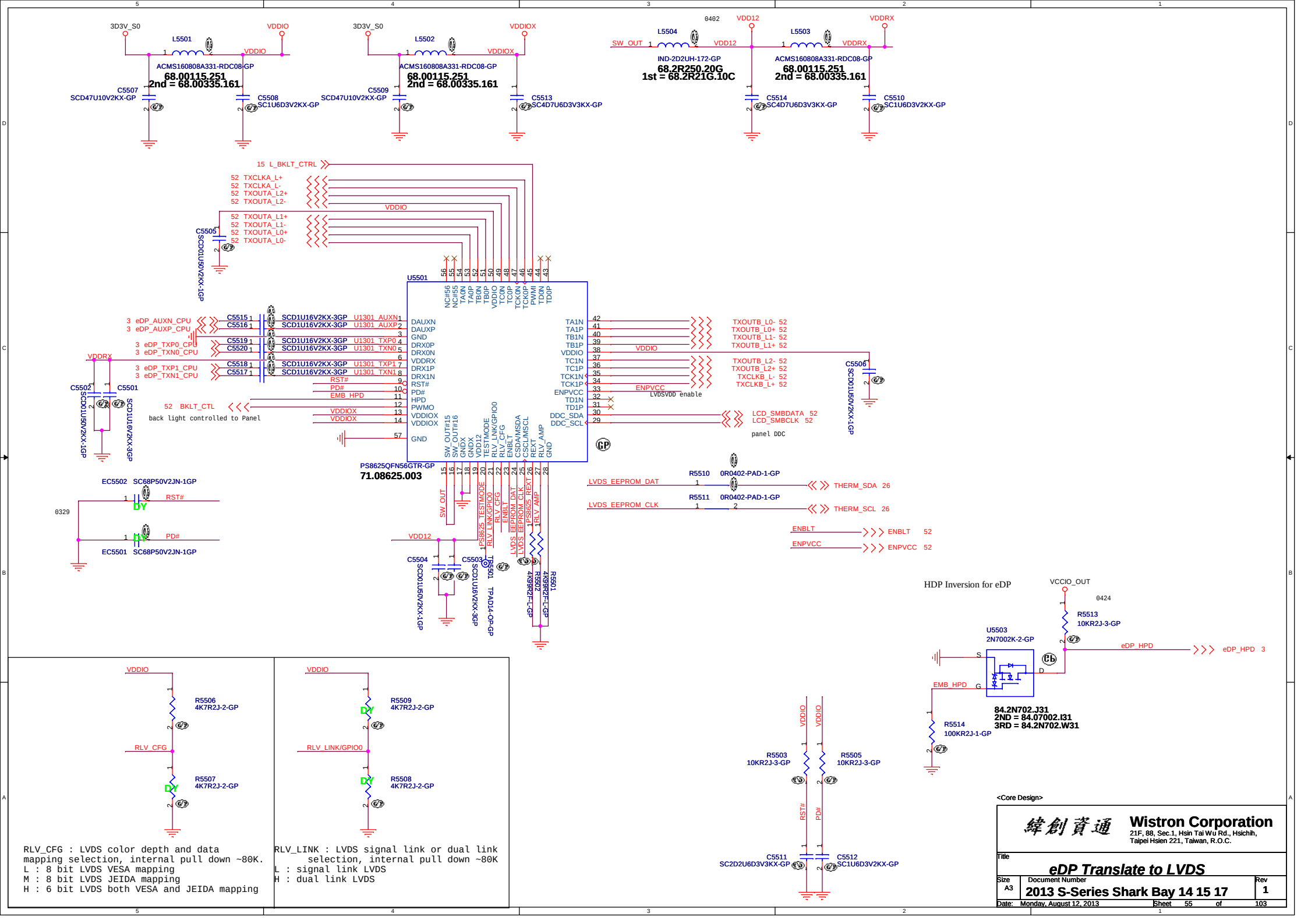
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

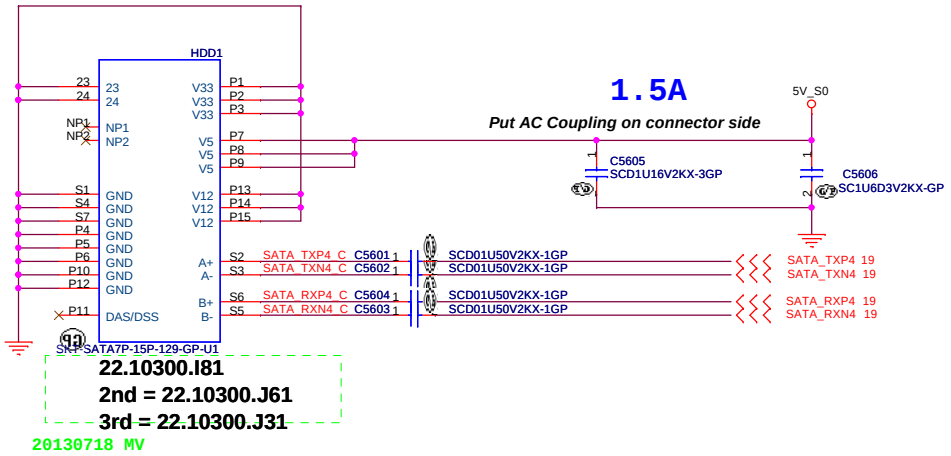
Title: **HDMI Level Shifter/Conn**

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 54 of 103

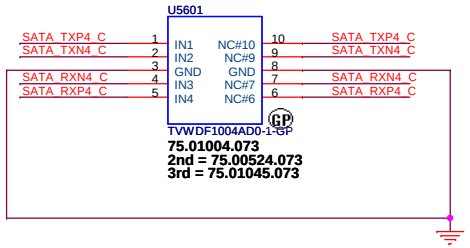

3D3V_S0
L5501
VDDIO
ACMS160808A331-RDC08-GP
68.00115.251
2nd = 68.00335.161
C5507
SCD47U10V2KX-GP
C5508
SC1U6D3V2KX-GP
3D3V_S0
L5502
VDDIOX
ACMS160808A331-RDC08-GP
68.00115.251
2nd = 68.00335.161
C5509
SCD47U10V2KX-GP
C5513
SC4D7U6D3V3KX-GP
0402
VDD12
VDDRX
L5504
L5503
SW_OUT
IND-2D2UH-172-GP
68.2R250.20G
1st = 68.2R21G.10C
ACMS160808A331-RDC08-GP
68.00115.251
2nd = 68.00335.161
C5514
SC4D7U6D3V3KX-GP
C5510
SC1U6D3V2KX-GP
15 L_BKLT_CTRL
52 TXCLKA_L+
52 TXCLKA_L-
52 TXOUTA_L2+
52 TXOUTA_L2-
VDDIO
52 TXOUTA_L1+
52 TXOUTA_L1-
52 TXOUTA_L0+
52 TXOUTA_L0-
C5505
SCD01U50V2KX-1GP
U5501
NC#56
NC#55
TA0N
TA0P
TB0N
TB0P
VDDIO
TC0N
TC0P
TCK0N
TCK0P
PWMI
TD0N
TD0P
3 eDP_AUXN_CPU
3 eDP_AUXP_CPU
3 eDP_TXP0_CPU
3 eDP_TXN0_CPU
3 eDP_TXP1_CPU
3 eDP_TXN1_CPU
C5515
C5516
C5519
C5520
C5518
C5517
SCD1U16V2KX-3GP
U1301_AUXN1
U1301_AUXP2
U1301_TXP0 4
U1301_TXN0 5
U1301_TXP1 7
U1301_TXN1 8
VDDRX
C5502
C5501
SCD01U50V2KX-1GP
SCD1U16V2KX-3GP
52 BKLT_CTL
back light controlled to Panel
RST#
PD#
EMB_HPD
VDDIOX
VDDIOX
GND
DAUXN
DAUXP
GND
DRX0P
DRX0N
VDDRX
DRX1P
DRX1N
RST#
PD#
HPD
PWMO
VDDIOX
VDDIOX
GND
SW_OUT#15
SW_OUT#16
GNDX
GNDX
VDD12
TESTMODE
RLV_LNK/GPIO0
RLV_CFG
ENBLT
CSDA/MSDA
CSCL/MSCL
REXT
RLV_AMP
GND
PS8625QFN56GTR-GP
71.08625.003
TA1N
TA1P
TB1N
TB1P
VDDIO
TC1N
TC1P
TCK1N
TCK1P
ENPVCC
TD1N
TD1P
DDC_SDA
DDC_SCL
ENPVCC
LVDSVDD enable
TXOUTB_L0- 52
TXOUTB_L0+ 52
TXOUTB_L1- 52
TXOUTB_L1+ 52
TXOUTB_L2- 52
TXOUTB_L2+ 52
TXCLKB_L- 52
TXCLKB_L+ 52
LCD_SMBDATA 52
LCD_SMBCLK 52
panel DDC
C5506
SCD01U50V2KX-1GP
EC5502 SC68P50V2JN-1GP
RST#
0329
PD#
EC5501 SC68P50V2JN-1GP
VDD12
C5504
C5503
SCD01U16V2KX-3GP
TP5501
TPAD14-OP-GP
SW_OUT
PS8625_TESTMODE
RLV_LNK/GPIO0
RLV_CFG
ENBLT
LVDS_EEPROM_DAT
LVDS_EEPROM_CLK
PS8625_REXT
RLV_AMP
R5502
4K69R2F-L-GP
R5501
LVDS_EEPROM_DAT
LVDS_EEPROM_CLK
R5510
0R0402-PAD-1-GP
R5511
0R0402-PAD-1-GP
THERM_SDA 26
THERM_SCL 26
ENBLT
ENBLT 52
ENPVCC
ENPVCC 52
HDP Inversion for eDP
VCCIO_OUT
0424
R5513
10KR2J-3-GP
U5503
2N7002K-2-GP
eDP_HPD
eDP_HPD 3
EMB_HPD
R5514
100KR2J-1-GP
84.2N702.J31
2ND = 84.07002.I31
3RD = 84.2N702.W31
VDDIO
R5506
4K7R2J-2-GP
RLV_CFG
R5507
4K7R2J-2-GP
RLV_CFG : LVDS color depth and data
mapping selection, internal pull down ~80K.
L : 8 bit LVDS VESA mapping
M : 8 bit LVDS JEIDA mapping
H : 6 bit LVDS both VESA and JEIDA mapping
VDDIO
R5509
4K7R2J-2-GP
RLV_LINK/GPIO0
R5508
4K7R2J-2-GP
RLV_LINK : LVDS signal link or dual link
selection, internal pull down ~80K
L : signal link LVDS
H : dual link LVDS
VDDIO
VDDIO
R5503
10KR2J-3-GP
R5505
10KR2J-3-GP
RST#
PD#
C5511
SC2D2U6D3V3KX-GP
C5512
SC1U6D3V2KX-GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
eDP Translate to LVDS
Size
A3
Document Number
2013 S-Series Shark Bay 14 15 17
Rev
1
Date: Monday, August 12, 2013
Sheet 55 of 103

HDD Connector

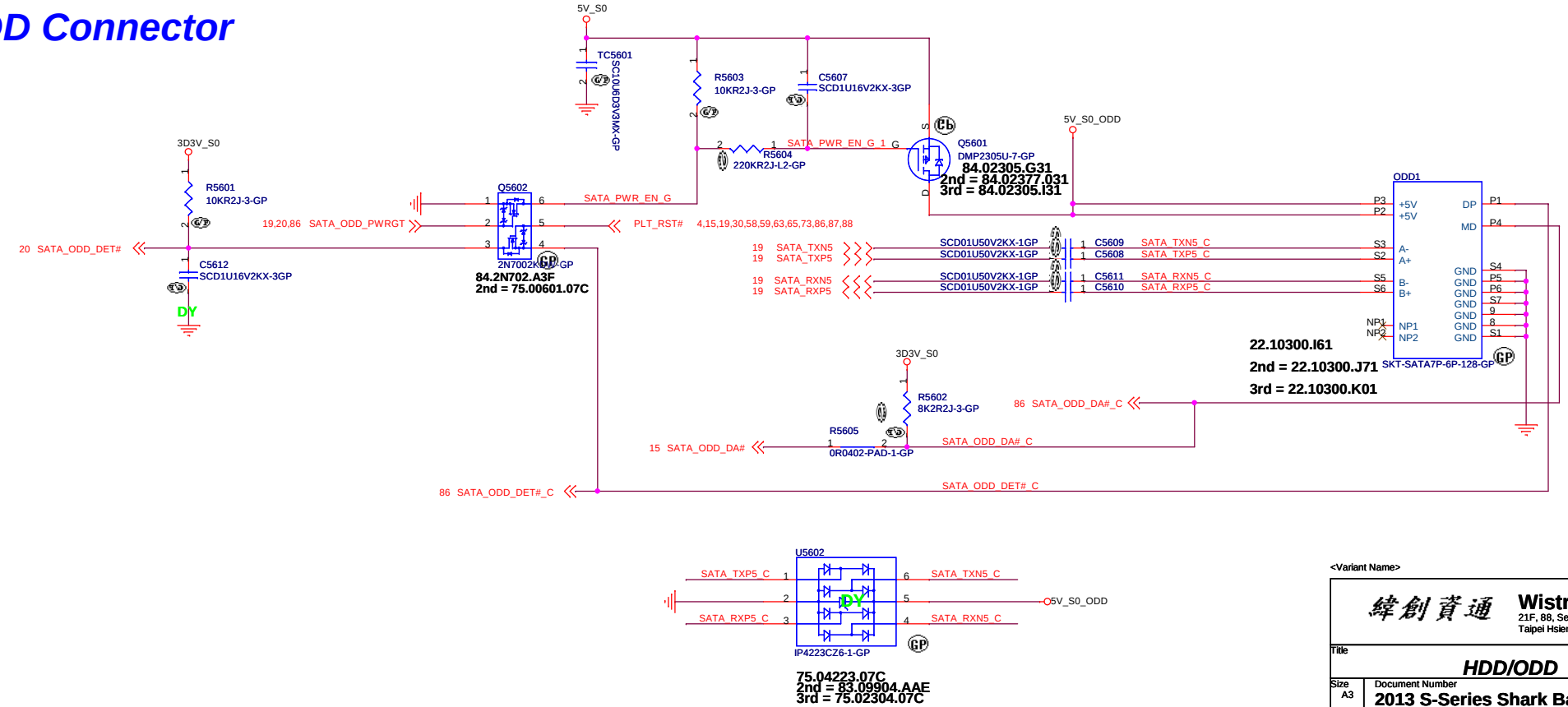


Ultra Low Capacitance TVS Arrays
(Pin5.6.7.8 No Internal Connection)

EMI Cap.



ODD Connector



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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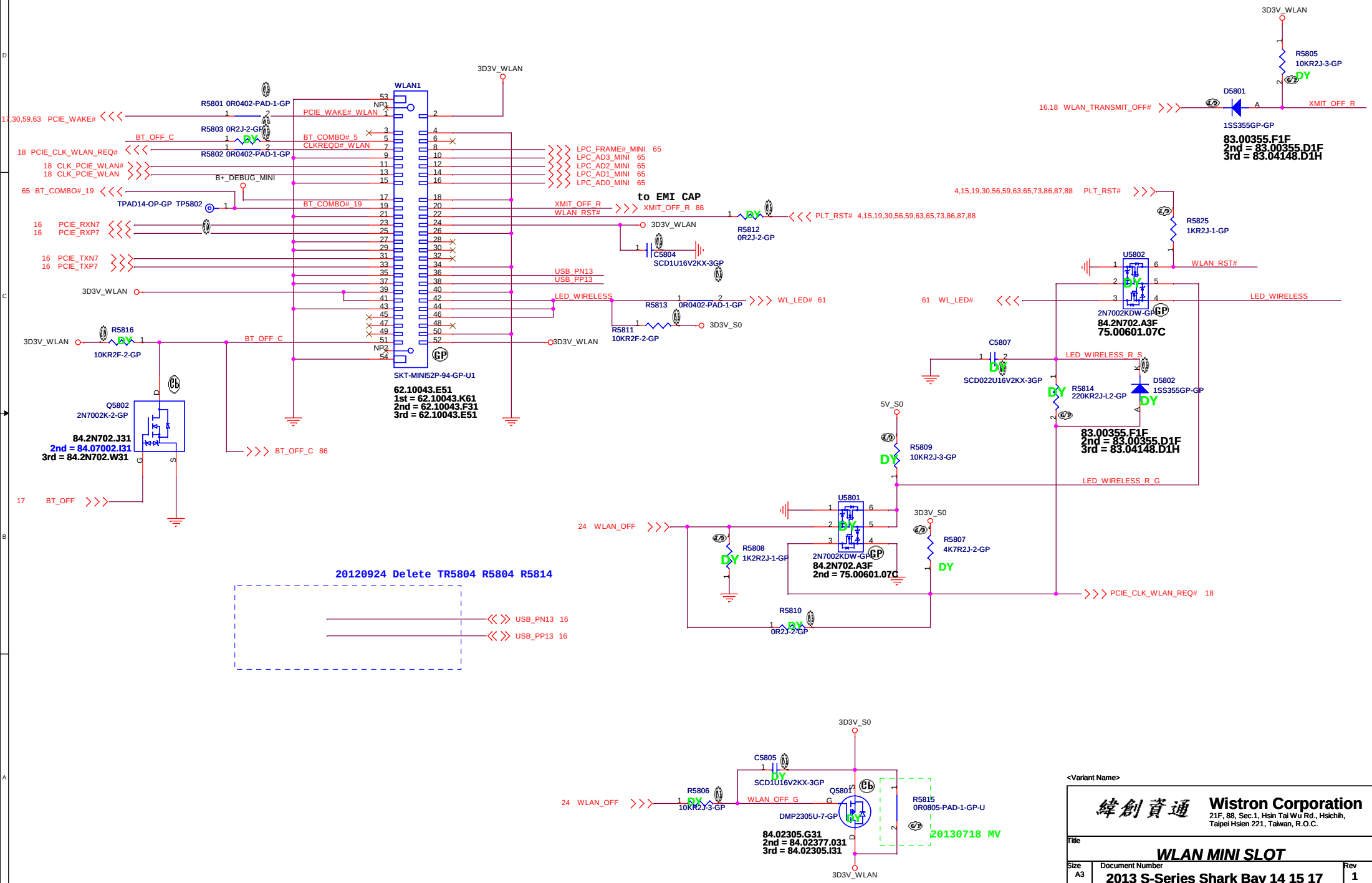
(Blanking)

WLAN Connector

Mini-Card--WLAN (Half)



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WLAN MINI SLOT

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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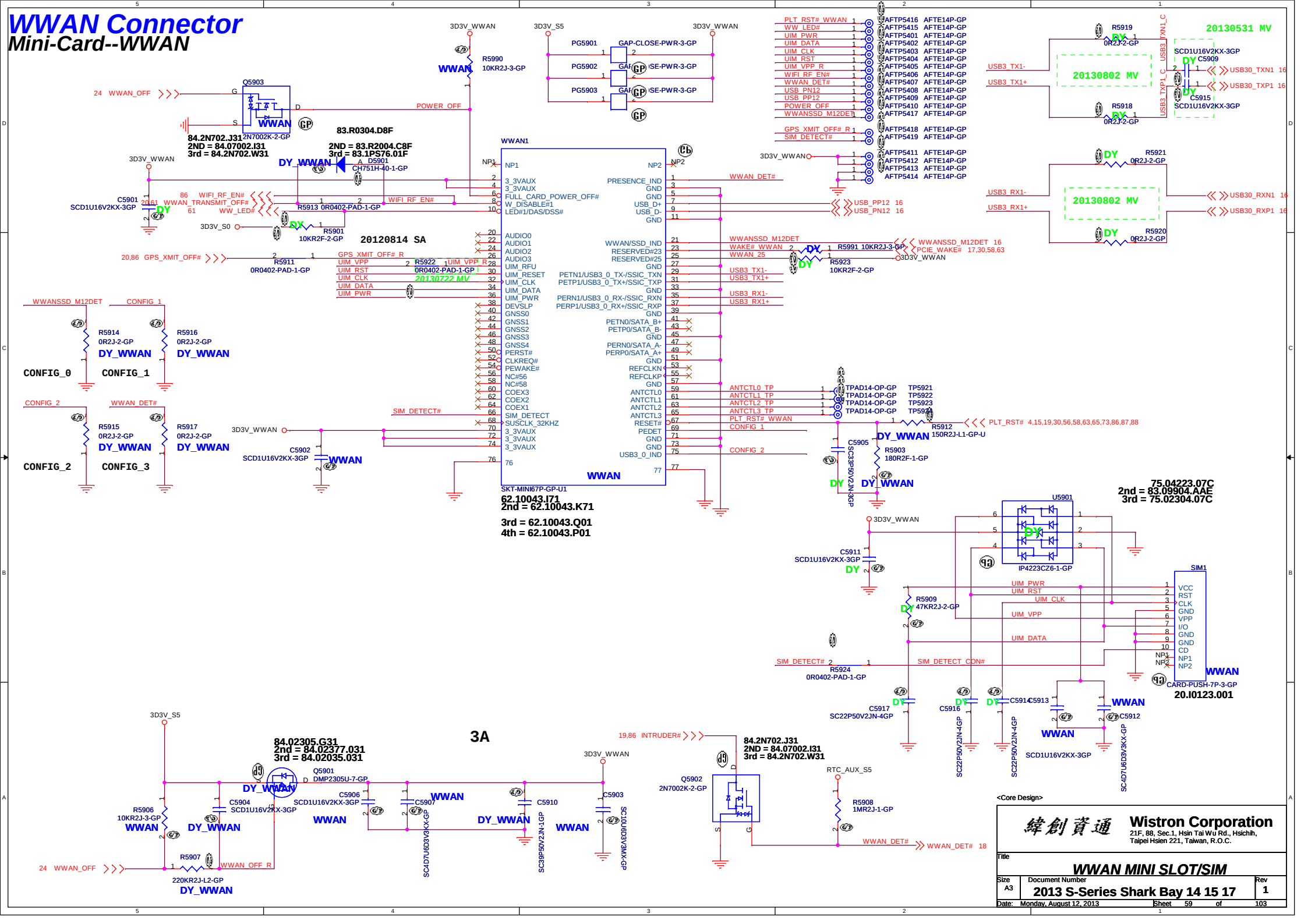
WWAN Connector
Mini-Card--WWAN



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **WWAN MINI SLOT/SIM**

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 59 of 103

<Variant Name>

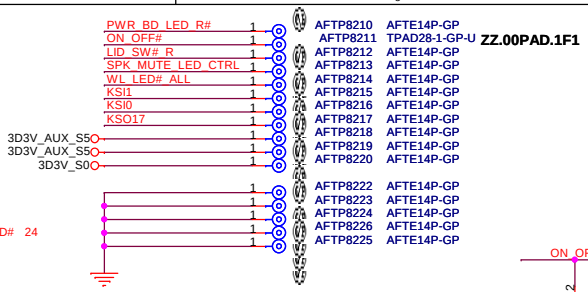
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

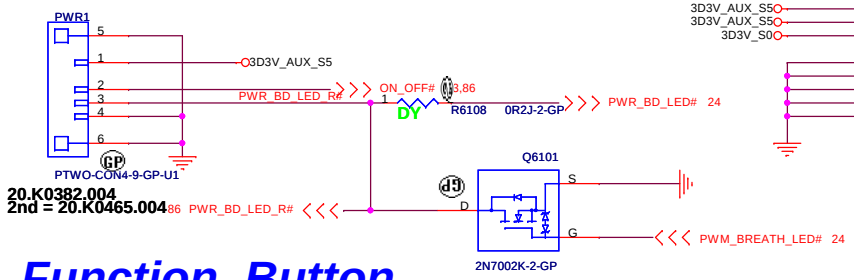
Title
Flash

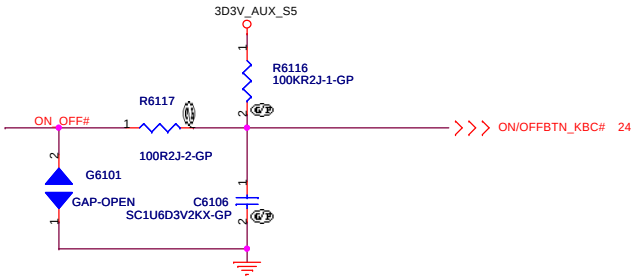
Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

Date: Wednesday, July 03, 2013 Sheet 60 of 103

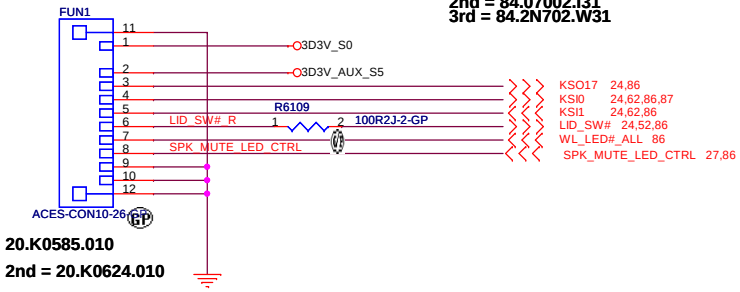
Power Button



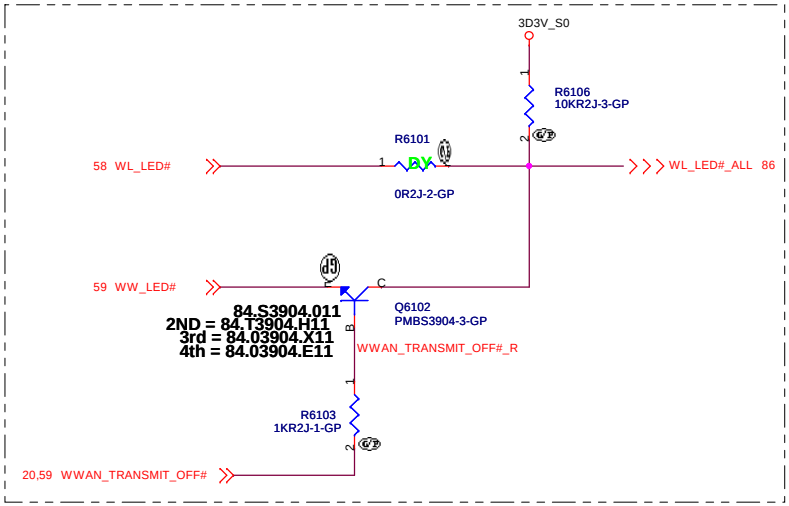


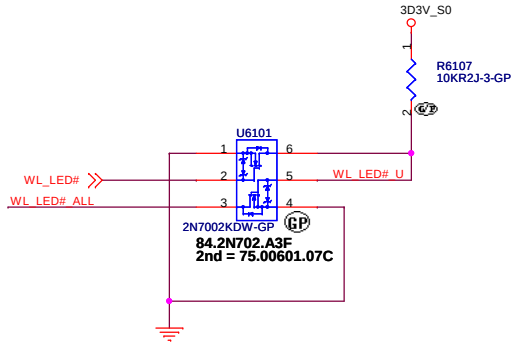


Function Button



WLAN / WWAN POWER LED





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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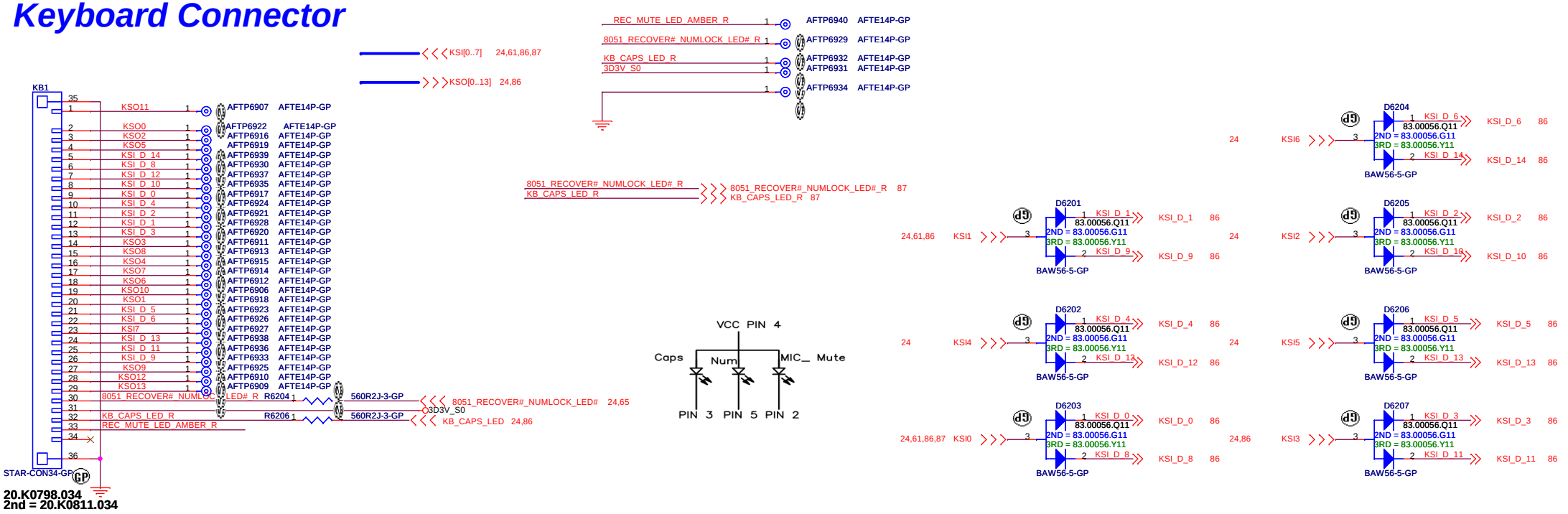
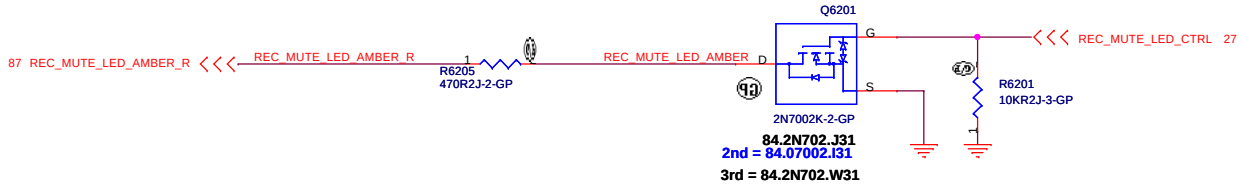
Keyboard Connector



20.K0798.034
2nd = 20.K0811.034

On Keyboard LEDs

<MUTE> Internal MIC ON= No light; OFF/Mute= Amber



84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31

<Core Design>

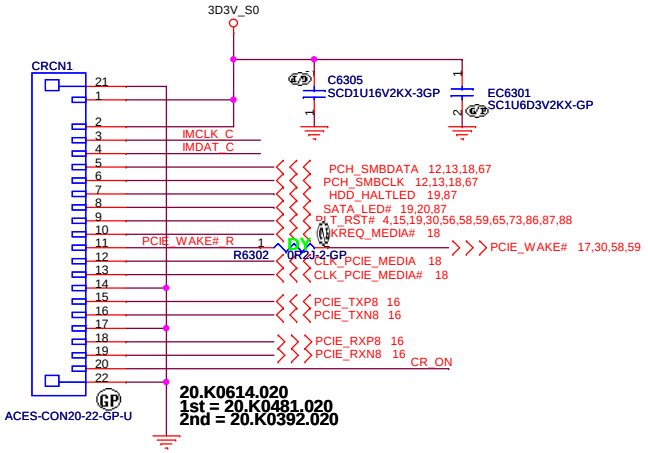
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Key Board/Touch Pad***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 62 of 103

Audio Board +Touch Pad + Card Reader IC Connector



PCIE_WAKE# 1 AFTP3127 AFTE14P-GP
CR_ON 1 AFTP3126 AFTE14P-GP

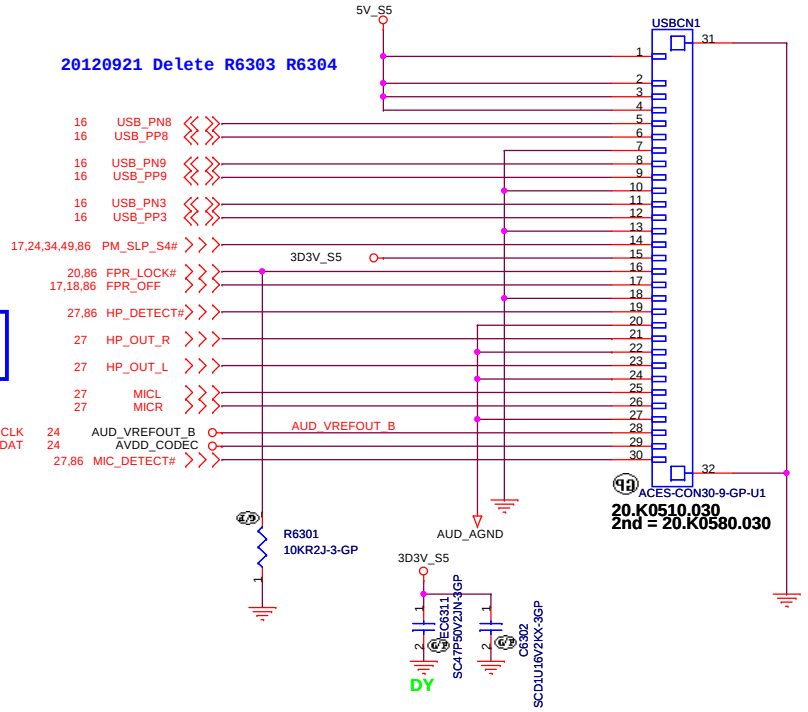
Fiji and Python no this function
Please connect to pin 11 pin20

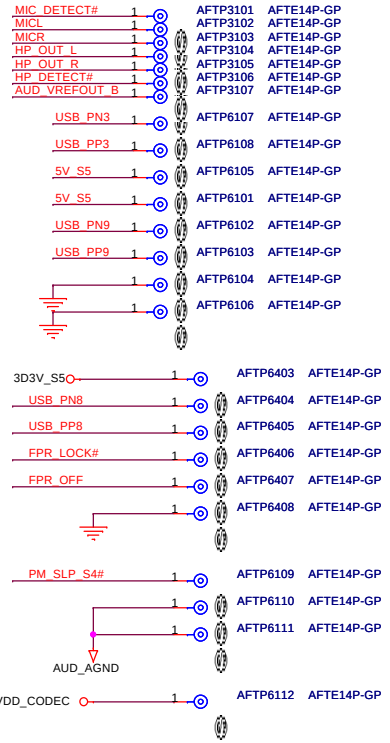
PCH_SMBDATA 1 AFTP3134 AFTE14P-GP
PCH_SMBCLK 1 AFTP3110 AFTE14P-GP
PLT_RST# 1 AFTP3108 AFTE14P-GP
CLKREQ_MEDIA# 1 AFTP3109 AFTE14P-GP
CLK_PCIE_MEDIA 1 AFTP3111 AFTE14P-GP
CLK_PCIE_MEDIA# 1 AFTP3112 AFTE14P-GP
PCIE_TXP8 1 AFTP3113 AFTE14P-GP
PCIE_TXN8 1 AFTP3114 AFTE14P-GP
PCIE_RXP8 1 AFTP3115 AFTE14P-GP
PCIE_RXN8 1 AFTP3116 AFTE14P-GP
HDD_HALTLED 1 AFTP3117 AFTE14P-GP
SATA_LED# 1 AFTP3118 AFTE14P-GP
IMCLK_C 1 AFTP3120 AFTE14P-GP
IMDAT_C 1 AFTP3121 AFTE14P-GP
3D3V_S0 1 AFTP3122 AFTE14P-GP
3D3V_S0 1 AFTP3123 AFTE14P-GP
1 AFTP3124 AFTE14P-GP
1 AFTP3125 AFTE14P-GP

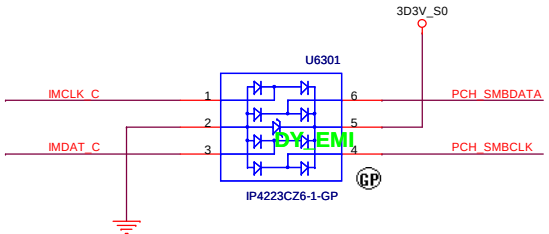
RN6302
IMCLK_C 1 4 IMCLK 24
IMDAT_C 2 3 IMDAT 24
0R4P2R-PAD

RN6301
3D3V_S0
IMCLK 2
IMDAT 1
4
SRN4K7J-8-GP

Right Side Audio & FP & USB Connector





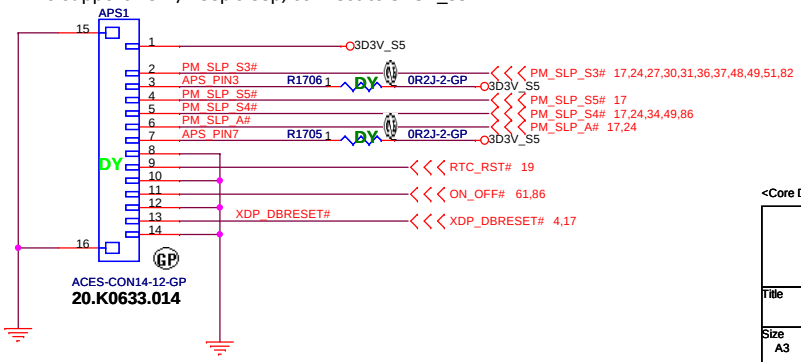


Pinout on customer's board,
as in the PDG, CDI #486713,

Pin	Signal Name
1	VccSus3_3
2	SLP_S3#
3	VccDSW3_3
4	SLP_S5#
5	SLP_S4#
6	SLP_A#
7	+V3.3DS
8	GND
9	RTCRST#
10	GND
11	PWRBTN#
12	GND
13	SYS_RESET#
14	GND

APS1 for QT test do not install

No support DSW/Deep sleep, connect to 3D3V_S5



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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<Variant Name>

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
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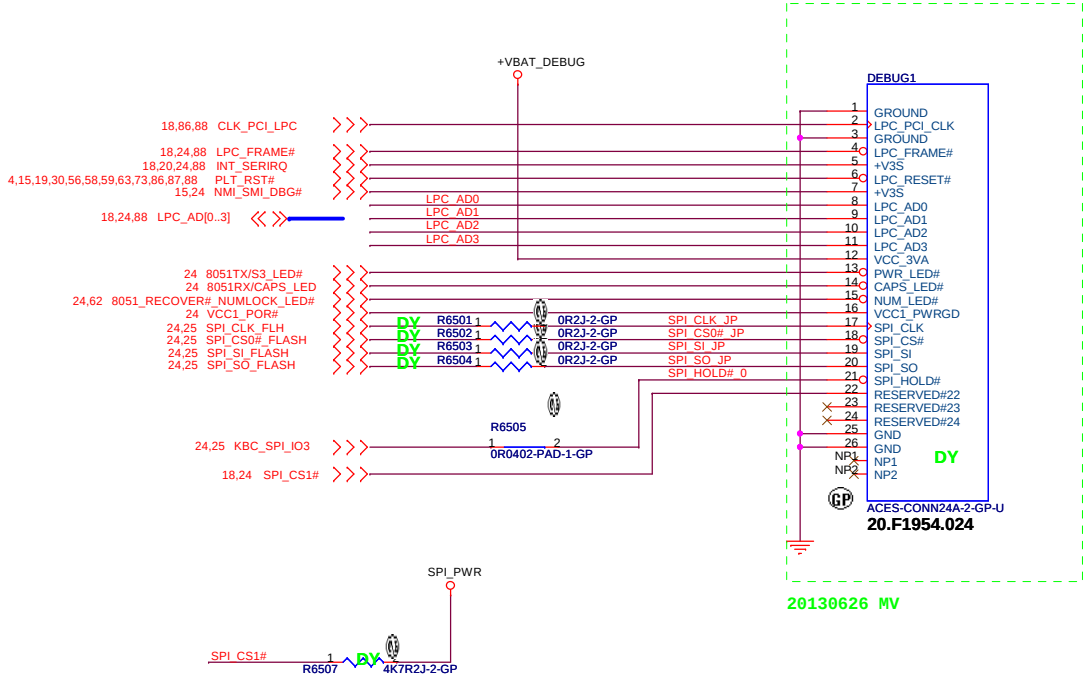
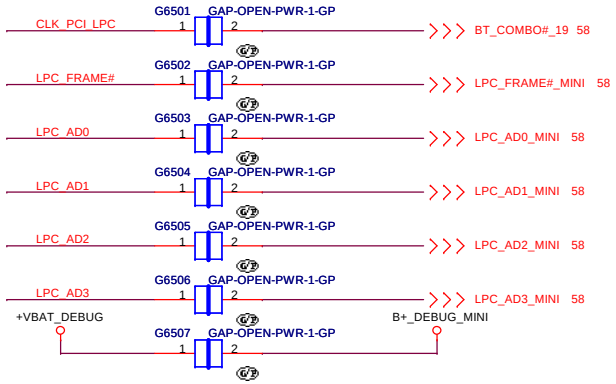
24 PIN LPC DEBUG CONN.



20130626 MV



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Dubug connector

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SENSOR HUB***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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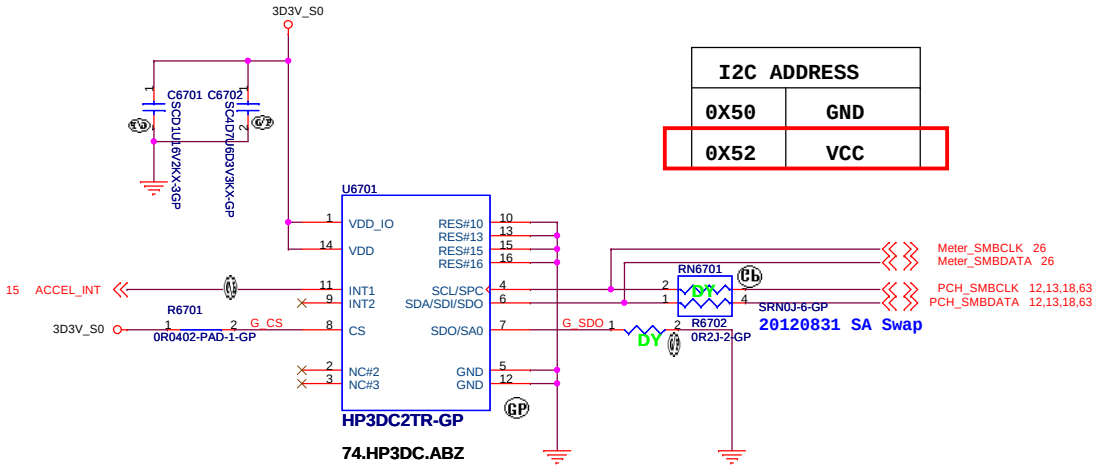
ACCELEROMETER



I2C ADDRESS	
0X50	GND
0X52	VCC

Must be placed in the center of the system

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***G Sensor***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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D C B A

5 4 3 2 1

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Thunderbolt (1/5)

Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

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<Variant Name>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Thunderbolt (2/5)

Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

Date: Wednesday, July 03, 2013 Sheet 69 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thunderbolt (3/5)***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Wednesday, July 03, 2013 Sheet 70 of 103

(Blanking)

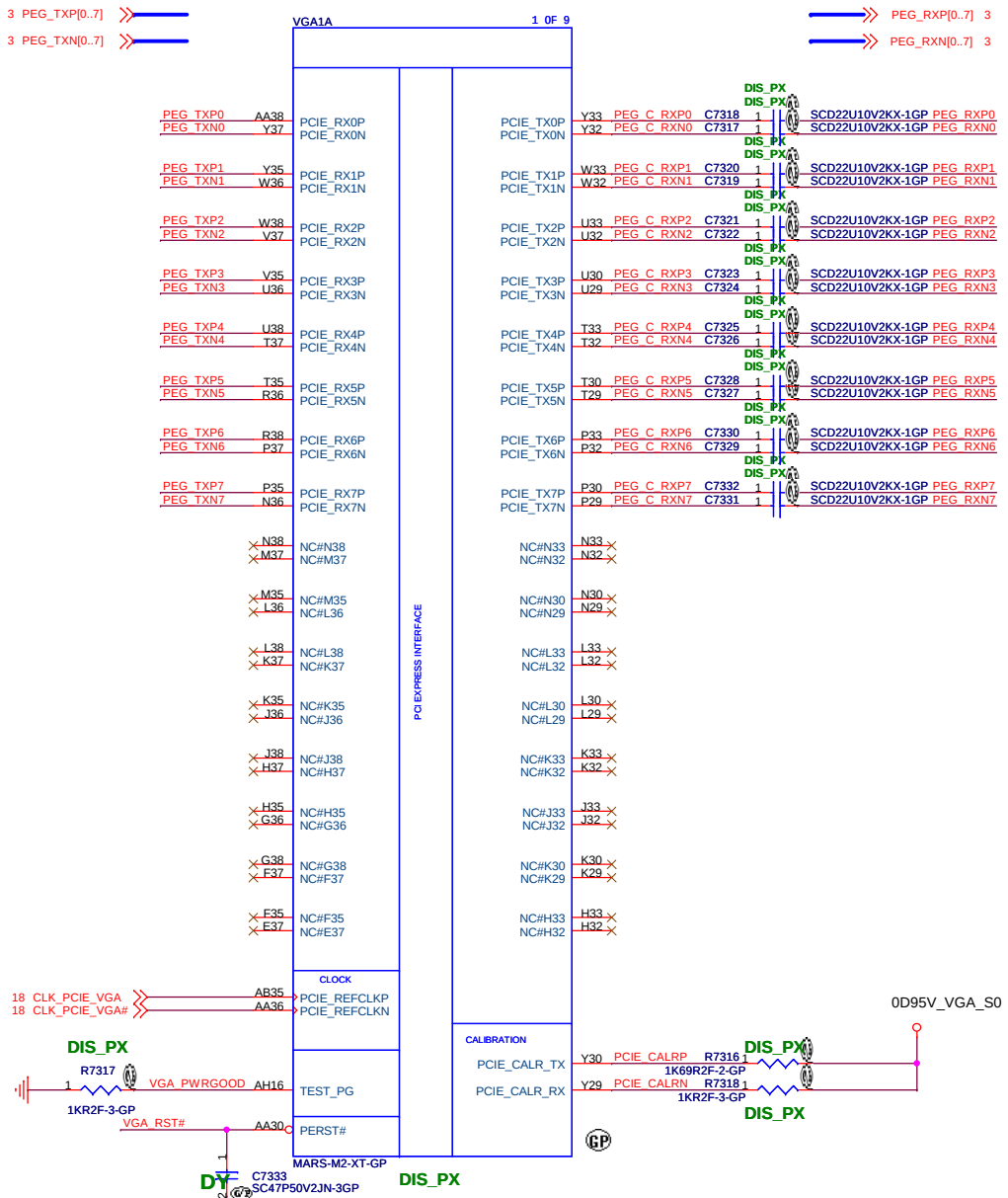
<Core Design>

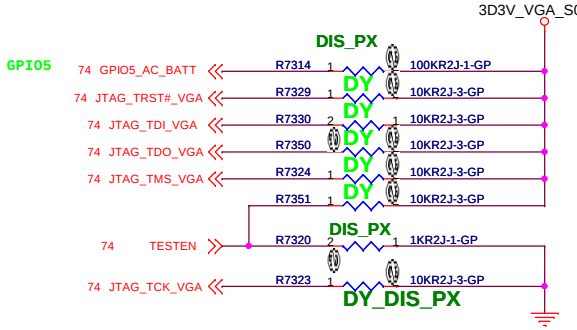
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thunderbolt (5/5)***

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14 15 17	1

Date: Wednesday, July 03, 2013 Sheet 72 of 103

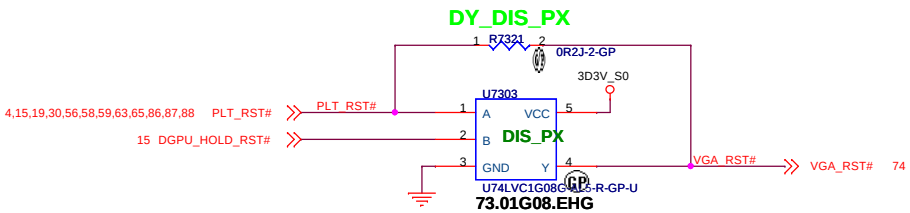




JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

dGPU reset for PX/SG transitions



73.01G08.EHG

2nd = 73.7SZ08.EAH
3rd = 73.01G08.L04

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (1/5) PEG

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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Set DVP as 1.8-V (VDDR4/5) general I/O

CTF setpoint is 118°C, and is programmed during ASIC initialization.

LVDS Interface

Close to VGA1

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

Intel is H_THERMTRIP#

VGA_PS3 VRAM Select
Check table for Select Resistor

MLPS Bit : PS_3[3:1]			R7427	R7426	Vendor & FN	Die	Process Tech	VRAM1	VRAM2
0	0	0	NC	4750	Samsung K4W1G1646G-BC11	G	35nm		
0	0	1	8450	2000	Samsung K4W2G1646E-BC1A	E	20nm	SI Stage	
0	1	0	4530	2000	Hynix H5TQ1G63EFR-11C	E	36nm		
0	1	1	6980	4990	Hynix H5TC2G63FFR-11C	F	25nm/JAN13		
1	0	1	3240	5620	Micron MT41J128M16JT-093G:K	K	30nm	SI Stage	
NC	NC	NC	3400	10000	UMA				

Vendor ID
00=Samsung
01=Hynix
10=Micron

0=64M
1=128M

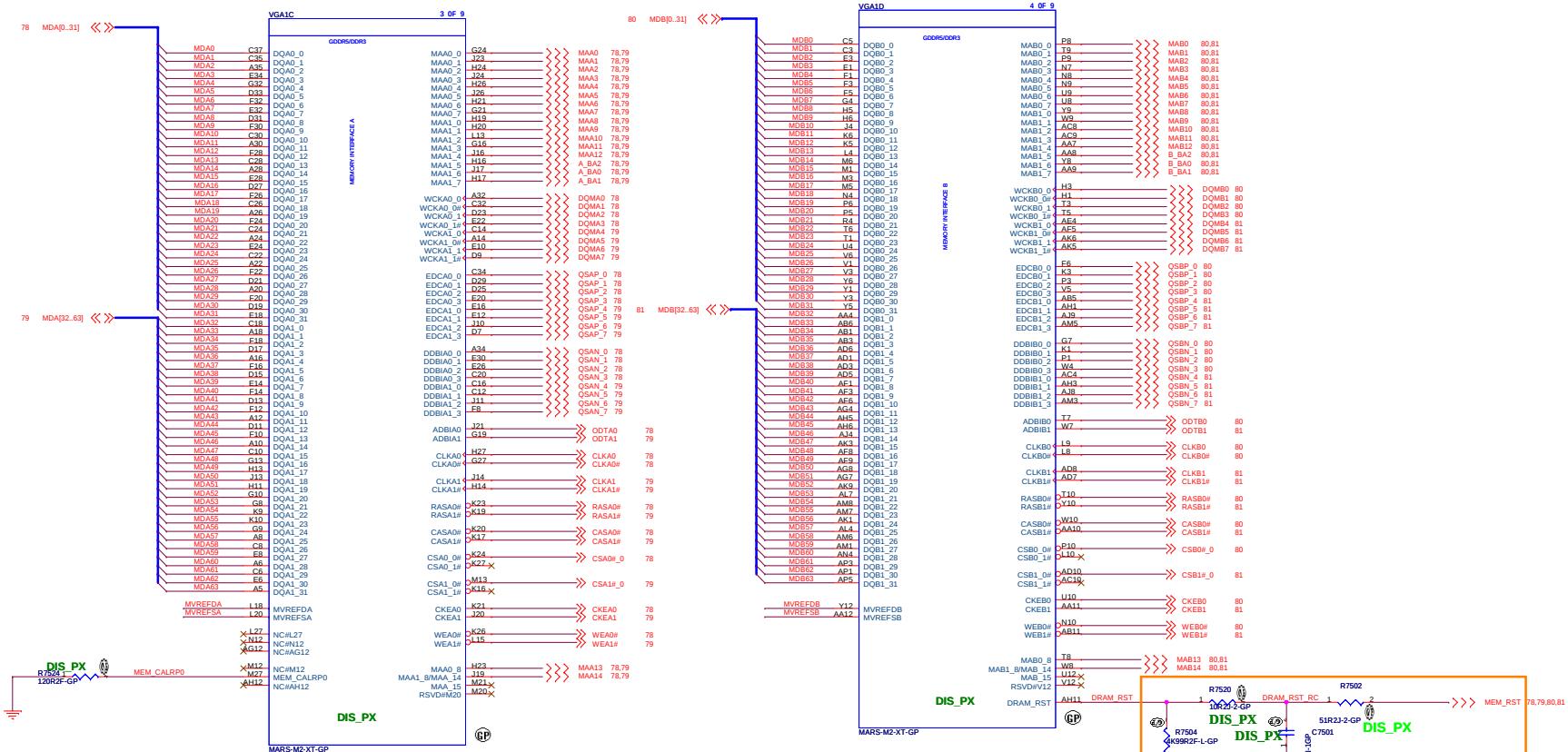
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

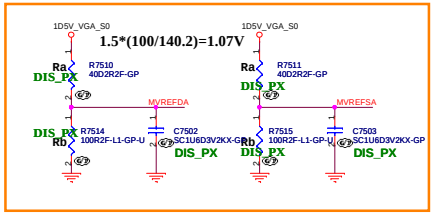
Title: GPU (2/5) DIGITALOUT

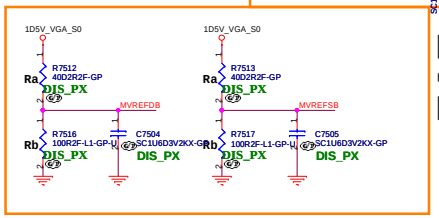
Size: A2 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 74 of 103



PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC





This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (3/5) VRAM I/F

Size: A2 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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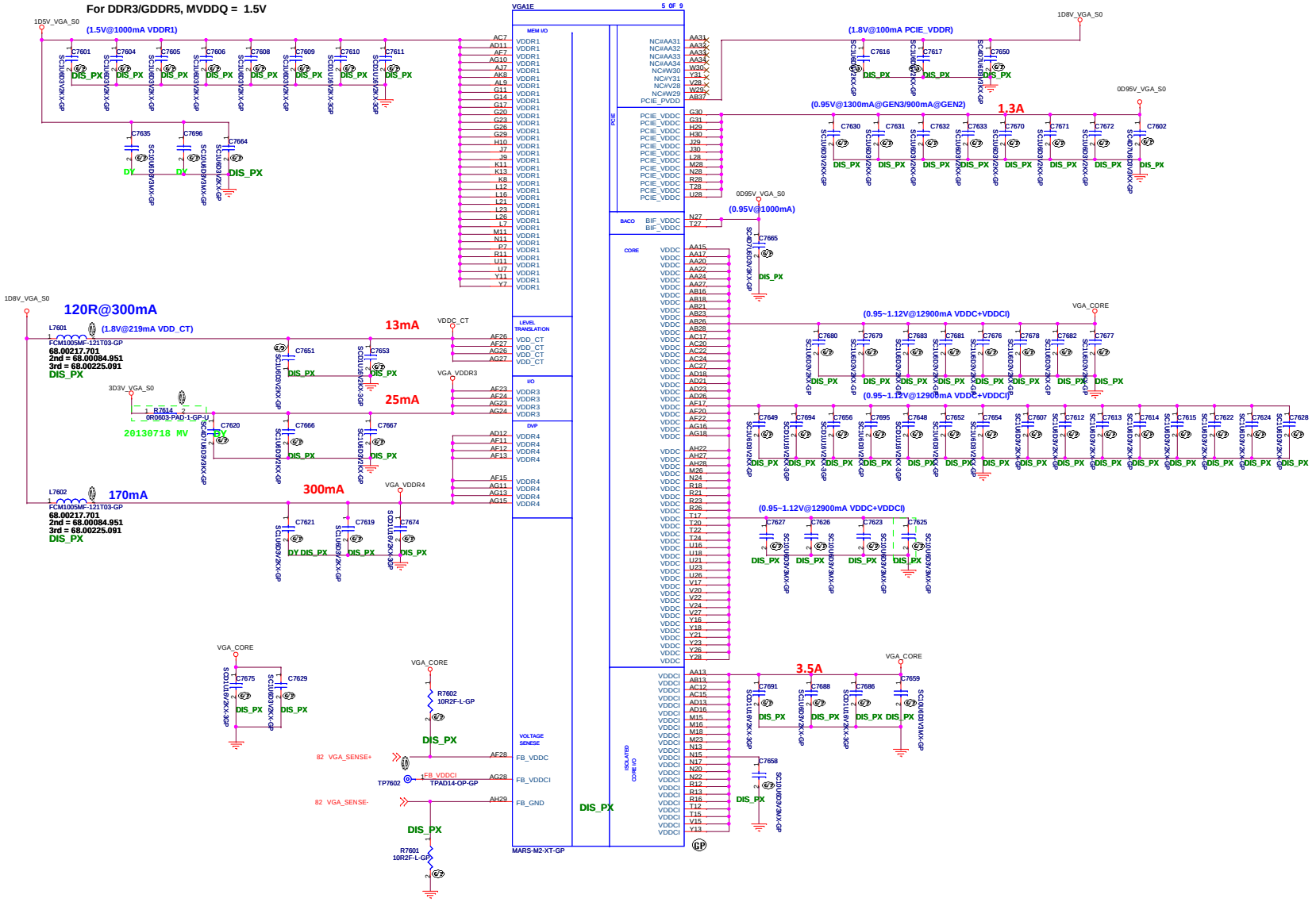

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (4/5) PWR

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14 15 17	1

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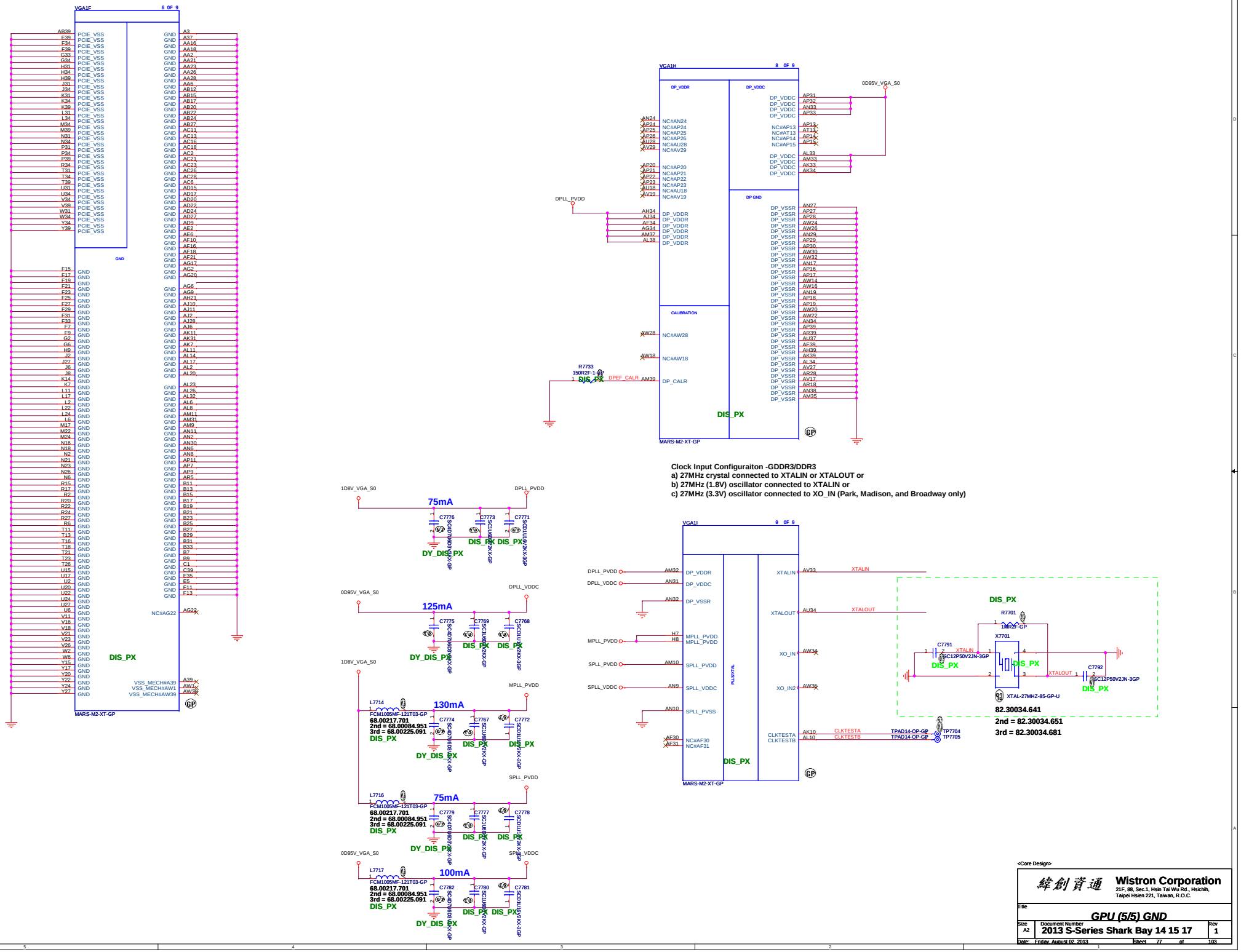


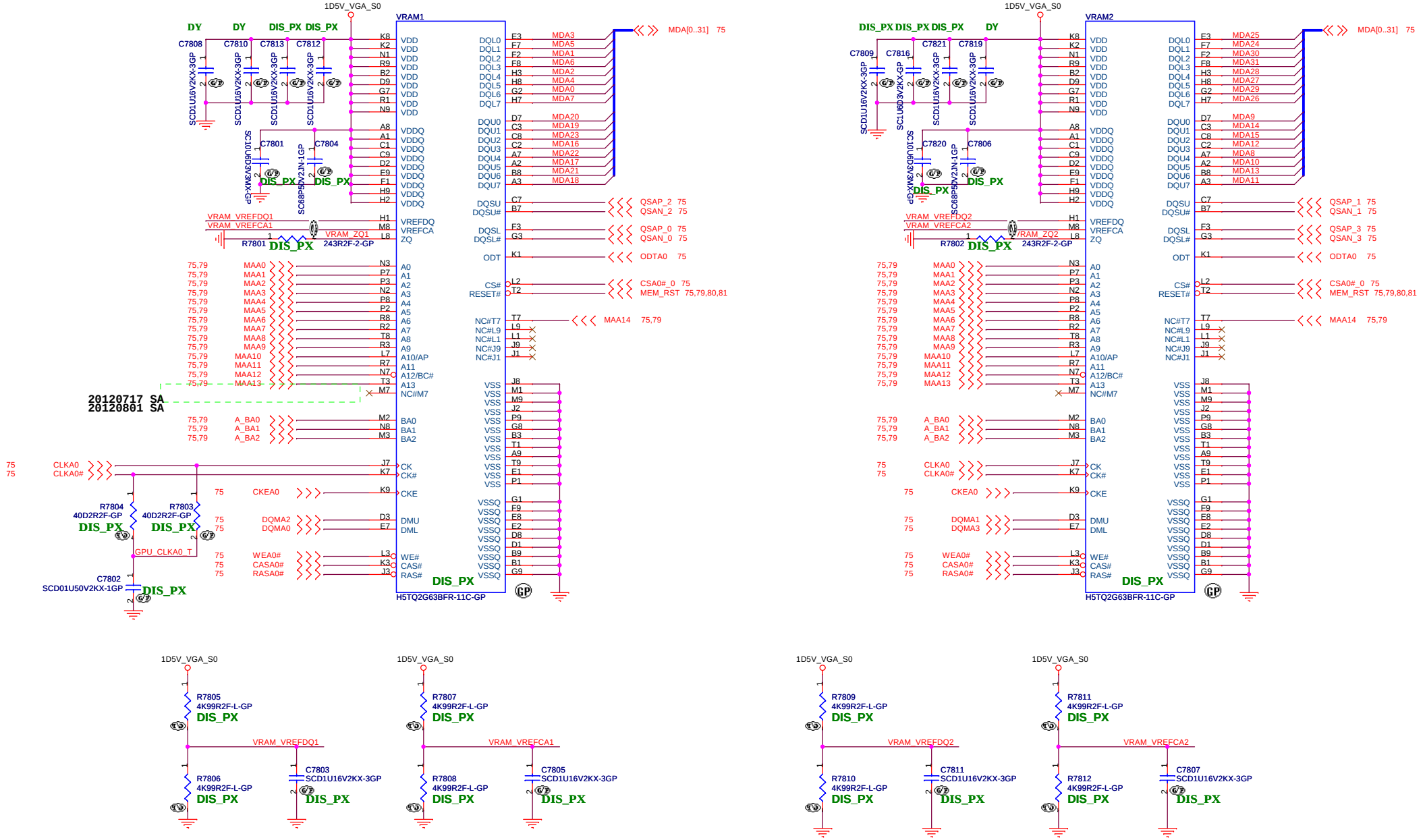
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU (5/5) GND**

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14 15 17	1

Date: Friday, August 02, 2013 Sheet 77 of 103



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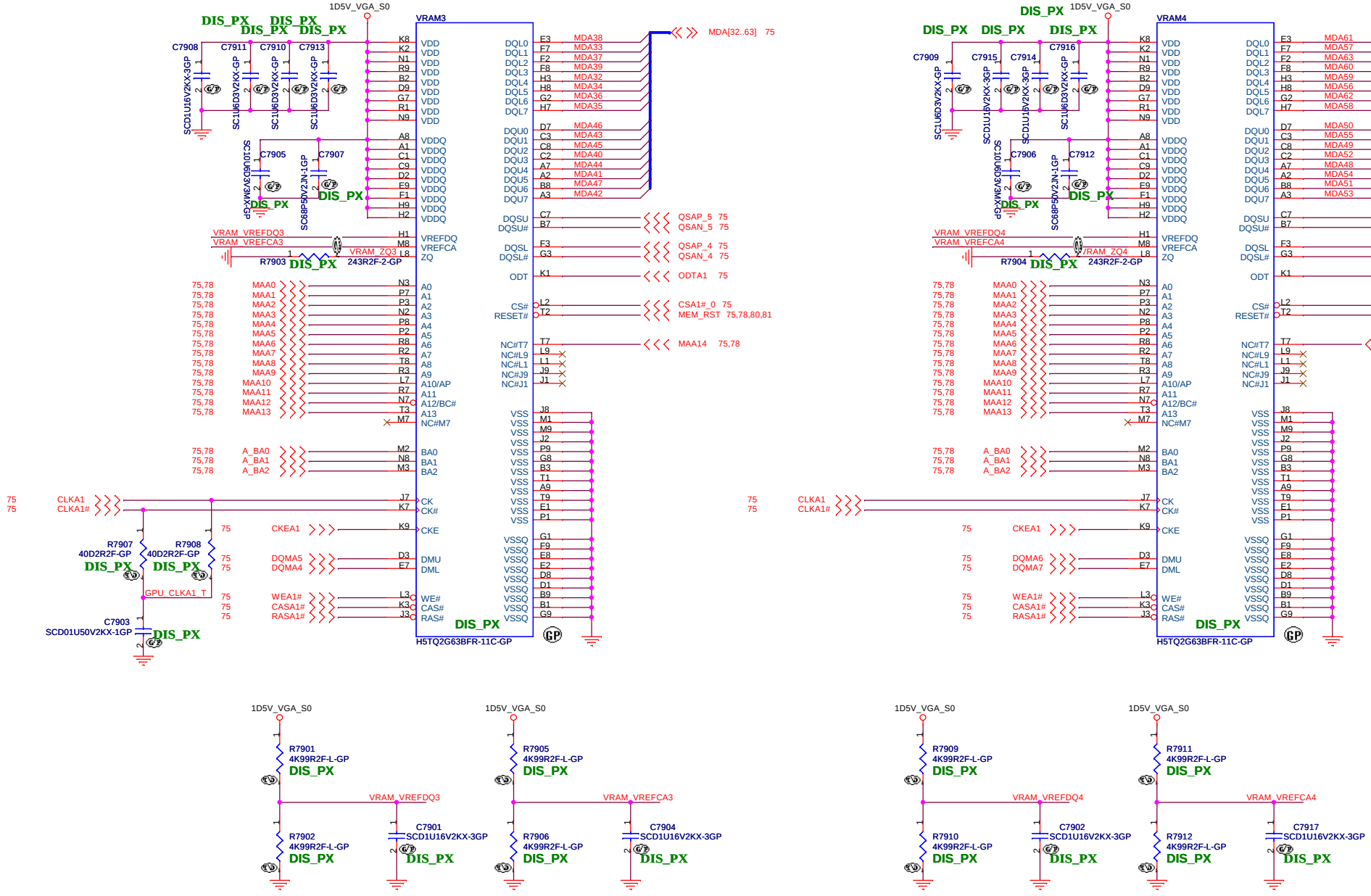
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM1,2 (1/4)**

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 78 of 103



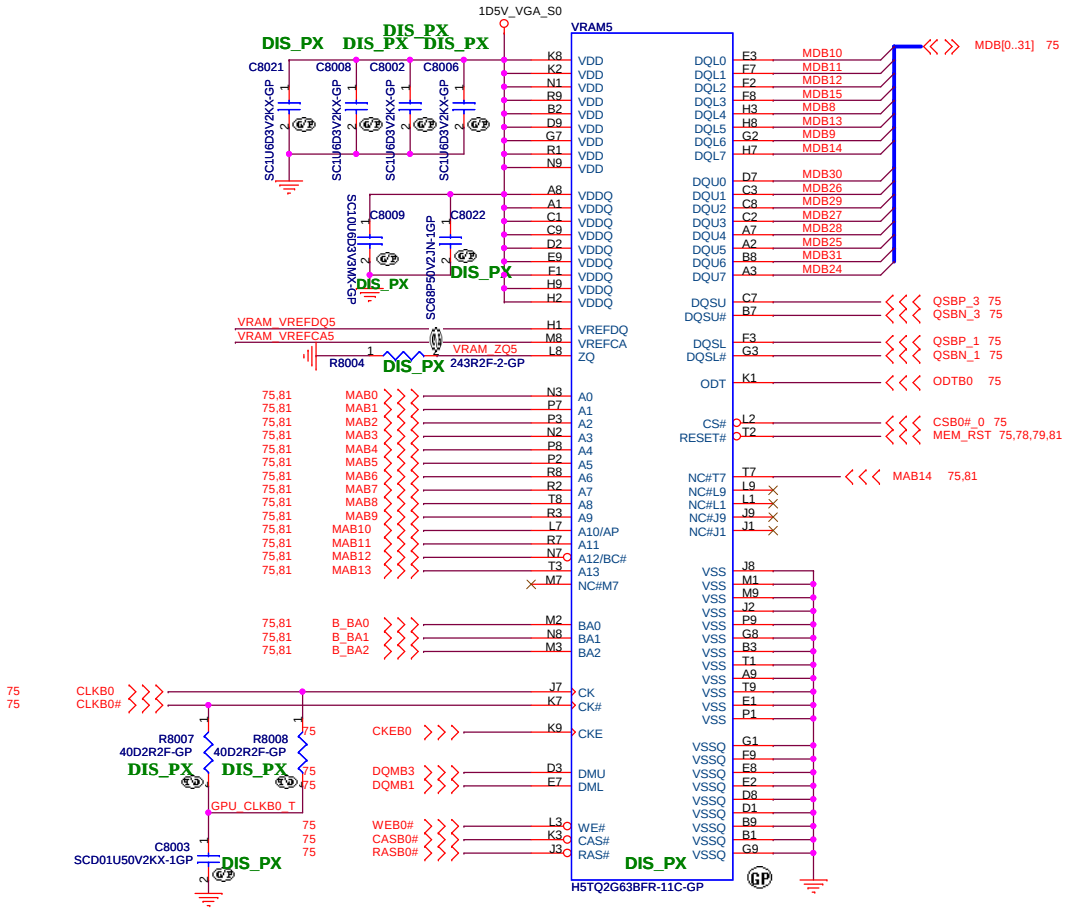
<Core Design>

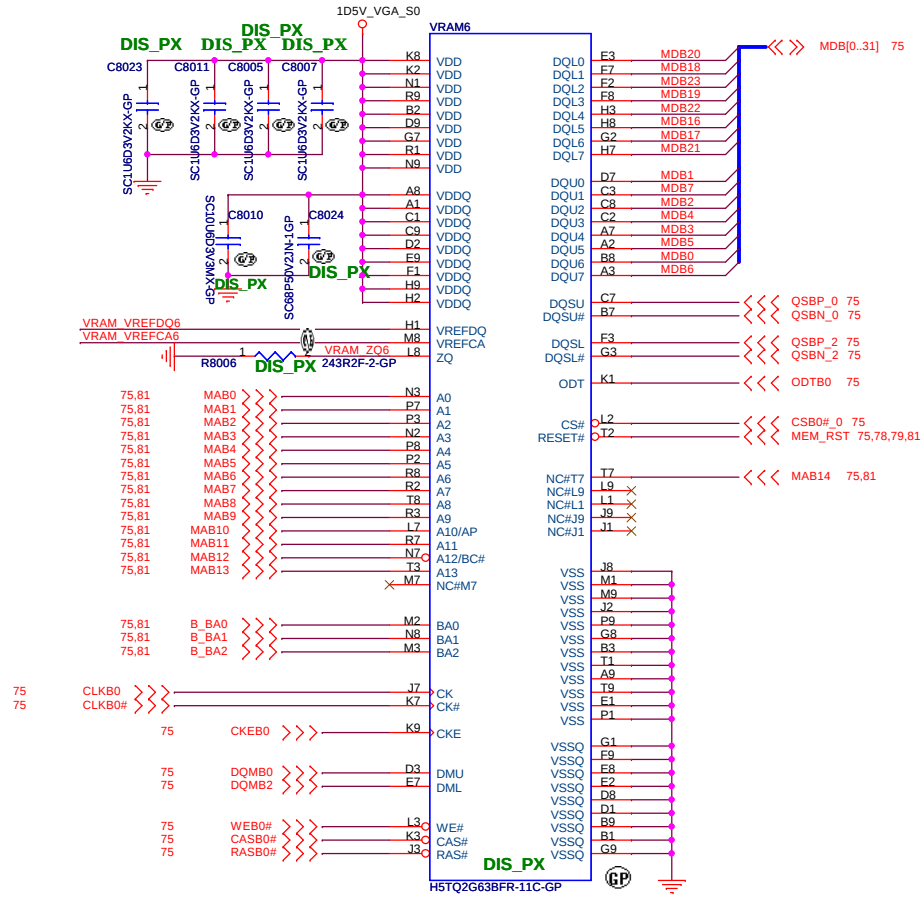
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

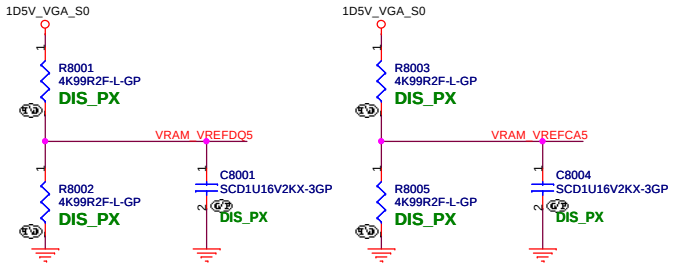
Title: VRAM3,4 (2/4)

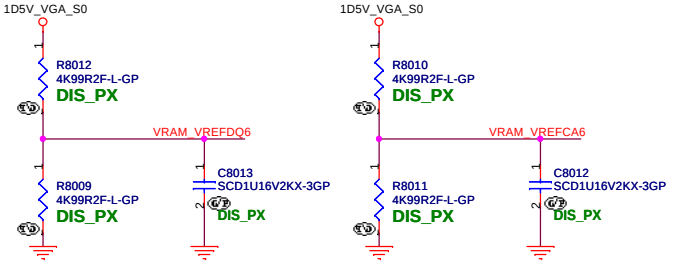
Size: A3 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

Date: Monday, August 12, 2013 | Sheet 79 of 103









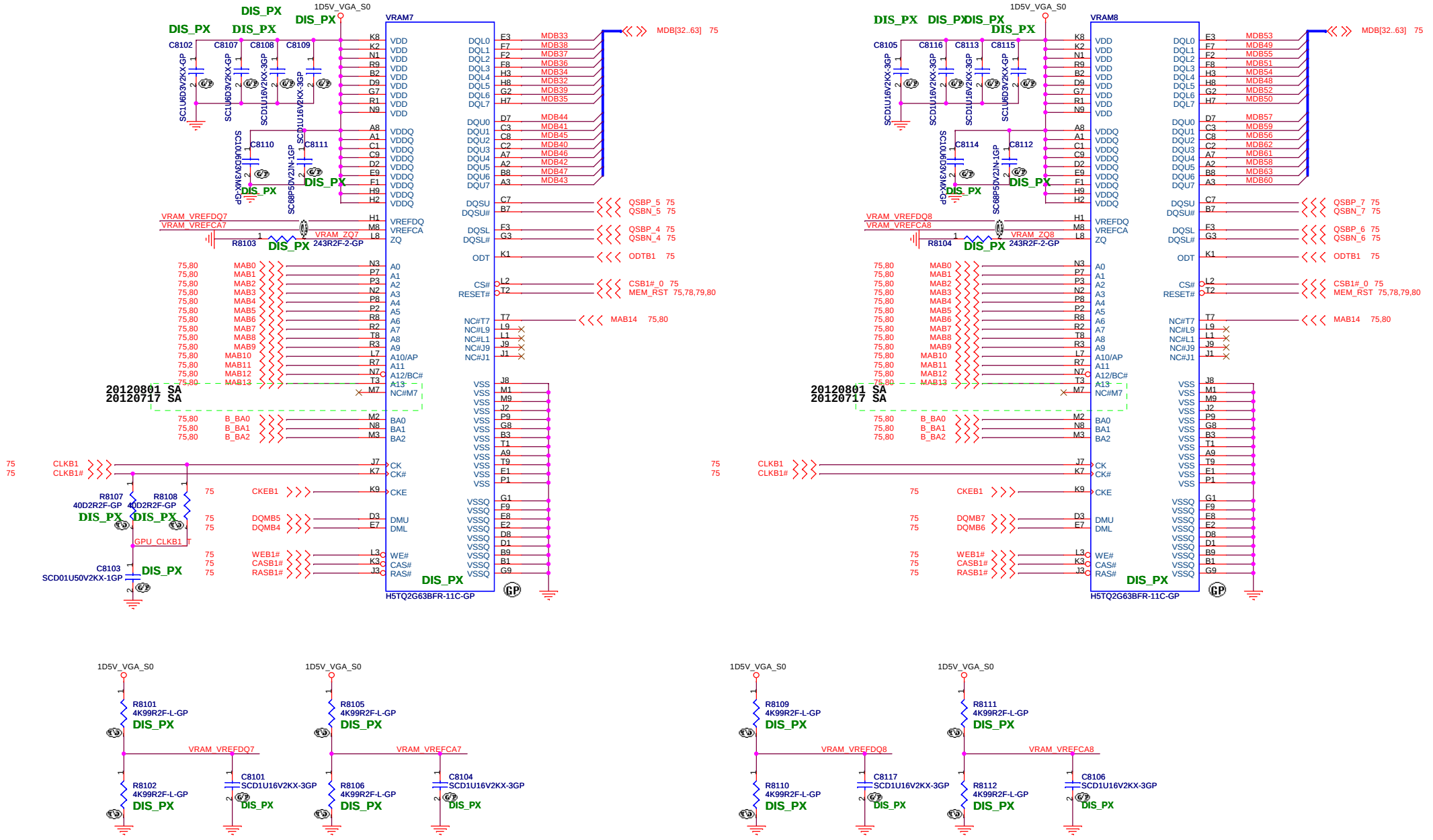
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM5,6 (3/4)**

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

Date: Monday, August 12, 2013 Sheet 80 of 103



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM7,8 (4/4)***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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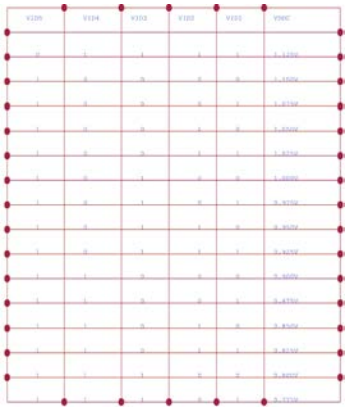
SSID = PWR.Plane.Regulator_vga_core

V-BOOT	VID0	VID1	VID2	VID3	VID4	VID5	VID6
0.85V	0	0	1	0	1	1	0



Design Current = 27A
OCP>55A

20121011 Delete R8201 C8201

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA_CORE

Size: A2 | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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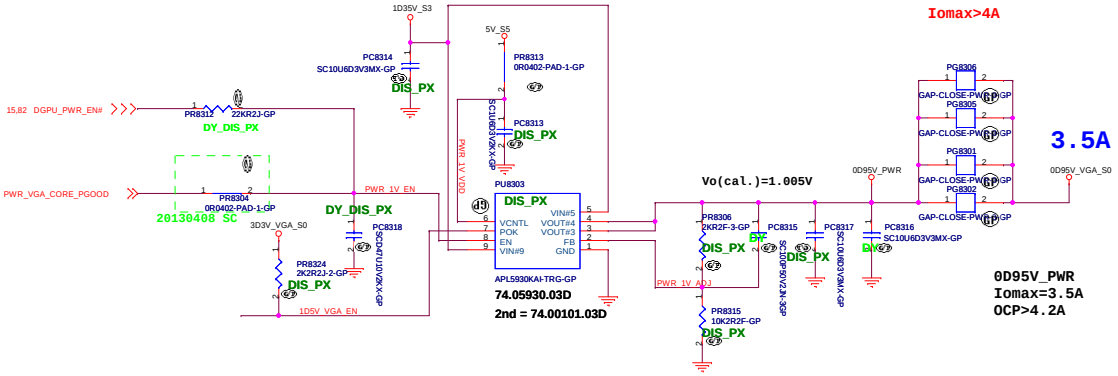
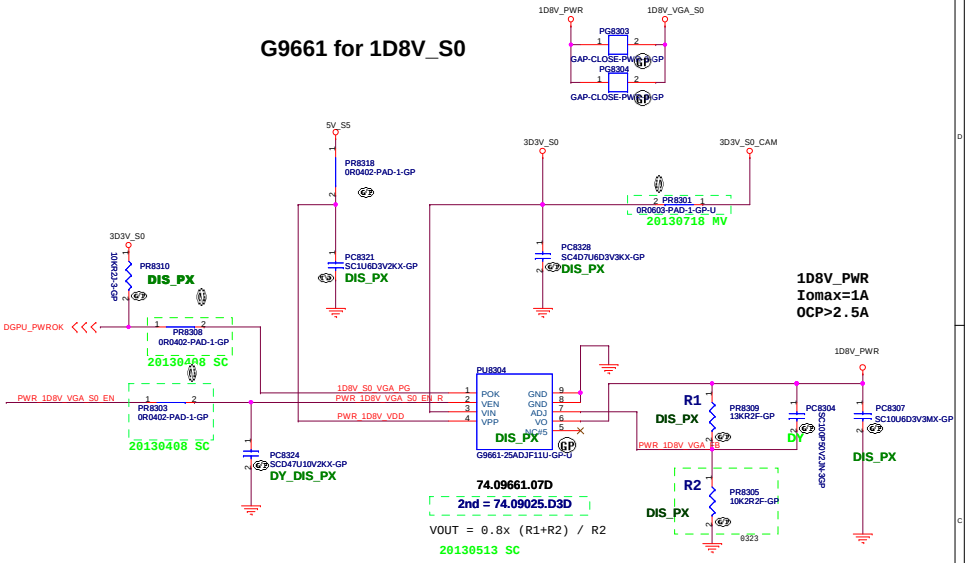
3D3V_VGA_S0 > VGA_CORE > 0D95V_VGA_S0 > 1D5V_VGA_S0 > 1D8V_VGA_S0

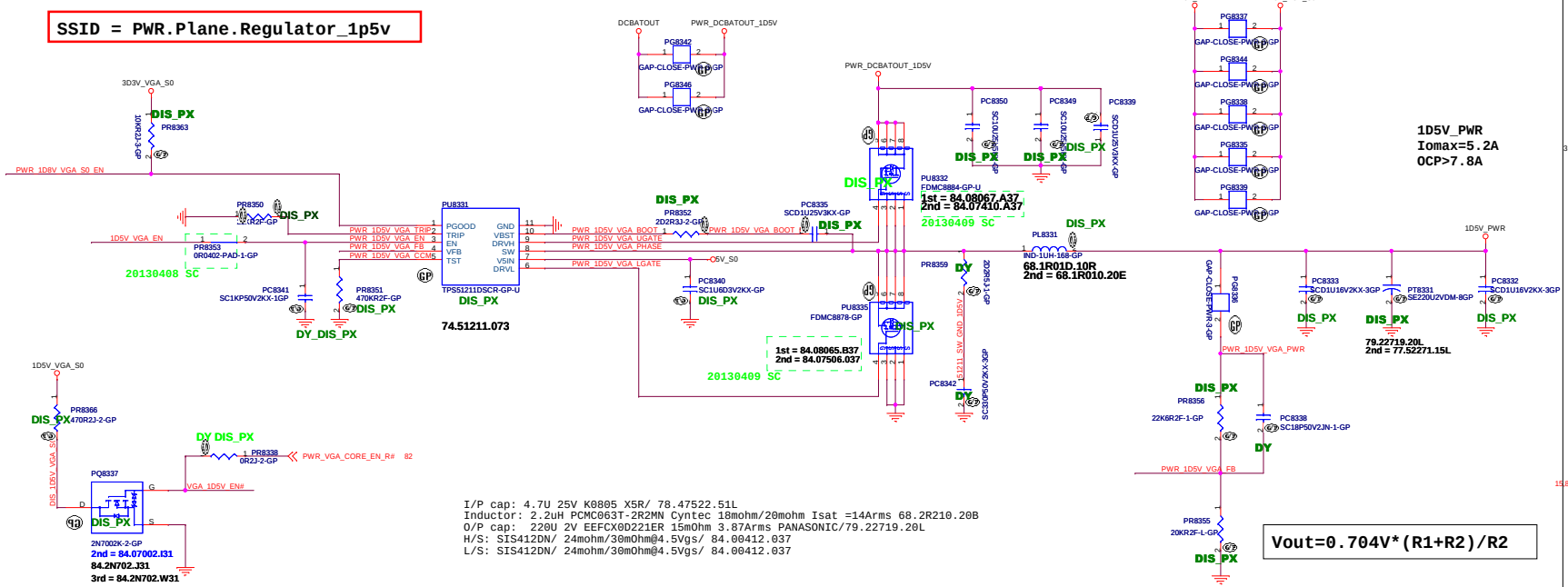
0D95V_S0



G9661 for 1D8V_S0

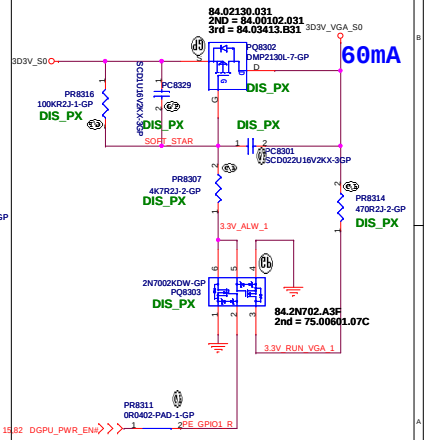


SSID = PWR.Plane.Regulator_1p5v



I/P cap: 4.7U 25V K0805 X5R/ 78.47522.51L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 3.87Arms PANASONIC/79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037

3D3V_VGA_S0



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14 15 17	1

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<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GPU Memory(2/5)***
Size: A2	Document Number: **2013 S-Series Shark Bay 1A 15 17** Rev: 1A
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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: 2013 S-Series Shark Bay 14/15/17 | Rev:

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CLOSE PU4005

CLOSE HDMI1

PAGE 17_PCH(1/9) 20130510 SC

PAGE 29_AUDIO CODEC EMI CAP

EC2904/EC2903 CLOSE U2901

20110626DB

PAGE 31_AUDIO CONNECTOR EMI CAP

CLOSE AUDIO1

PAGE 34_Lan RTL8111E EMI CAP

CLOSE U3401 Pin25

PAGE 35_LAN RJ45 EMI CAP

PAGE 39_BATT CONN EMI CAP

PAGE 49_LVDS EMI CAP

PUT CLOSE R4911

20120727 SA

PAGE 57_CRT EMI CAP

20121130 SB

PAGE 50_CRT EMI CAP

PAGE 51_HDMI EMI CAP

PAGE 53_WLAN SLOT EMI CAP

PAGE 54_WLAN SLOT EMI CAP

CLOSE WWAN1

PAGE 56_HDD/ODD EMI CAP

20121130 SB

PAGE 61_USB2.0 EMI CAP

CLOSE USB21

PAGE 61 62_USB3.0 EMI CAP

near USBCN1

near USB2 / USB3

20121130 SB

PAGE 64_FINGER PRINT EMI CAP

PAGE 82_DCIN EMI CAP

CLOSE FUN1

CLOSE PWR1

20130116 SB

PAGE 40-48,92_POWER EMI CAP

CLOSE TO PU4005

CLOSE TO PU4303

CLOSE TO PU4401

CLOSE TO PU4501

CLOSE TO PU4601

CLOSE TO PU4701

PAGE 21

Put Caps near DIMMA1

Put Caps near DIMMA2

20120713 SA

PU4101

PU4102

PAGE 69_KEYBOARD/TOUCH PAD EMI CAP

20130116 SB

20120919 SA

CLOSE TO PU9202

20130507 SC

20121005 SA

PAGE 62_USB3.0 CAP

CLOSE USBCN1

CLOSE USB2

CLOSE USB3

CLOSE U6204

CLOSE U6205

20130730 MV

<Core Design>

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size: Custom | Document Number: 2013 S-Series Shark Bay 14 15 17 | Rev: 1

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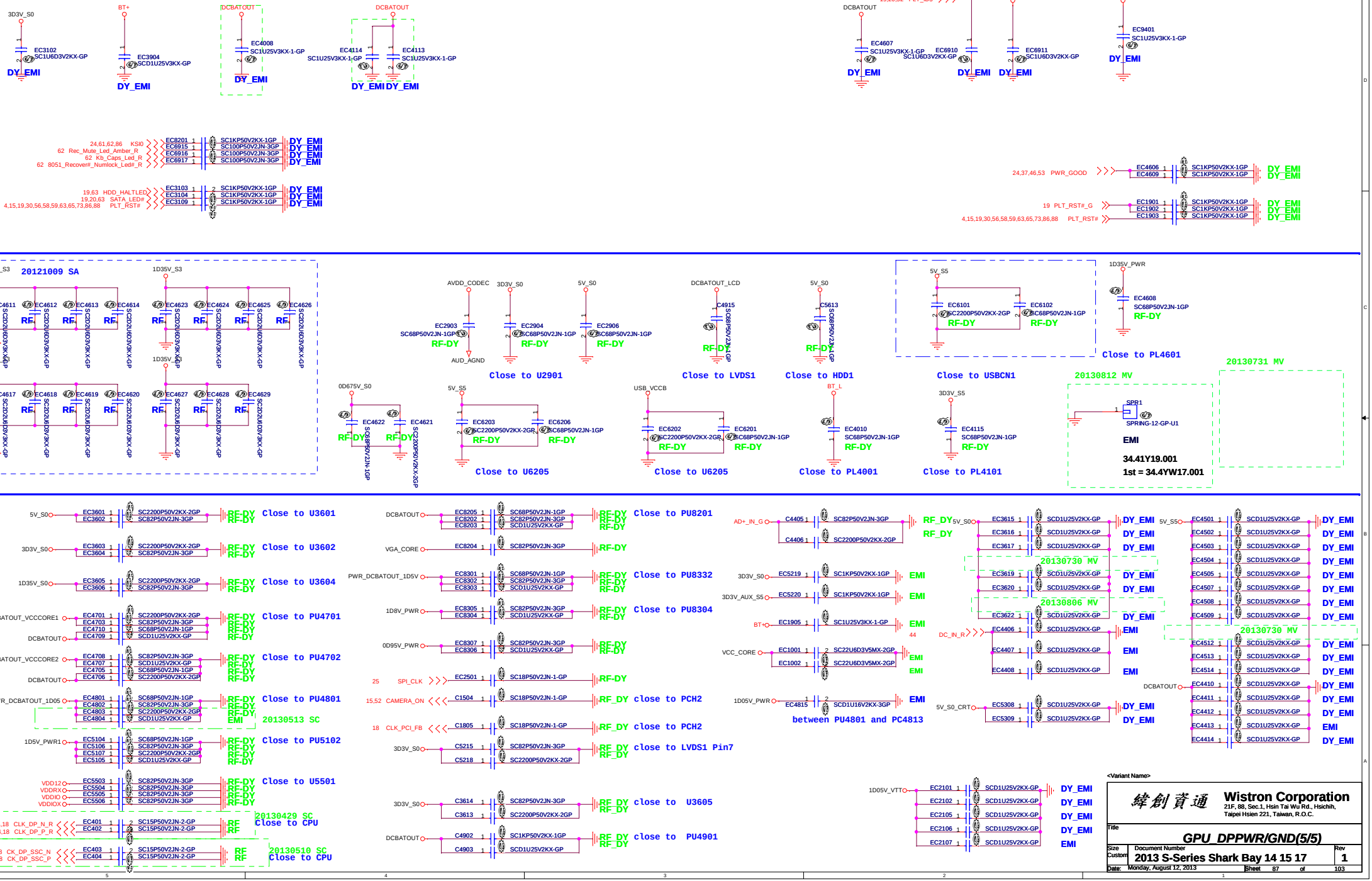
EMI Caps



<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
Custom	2013 S-Series Shark Bay 14 15 17	1

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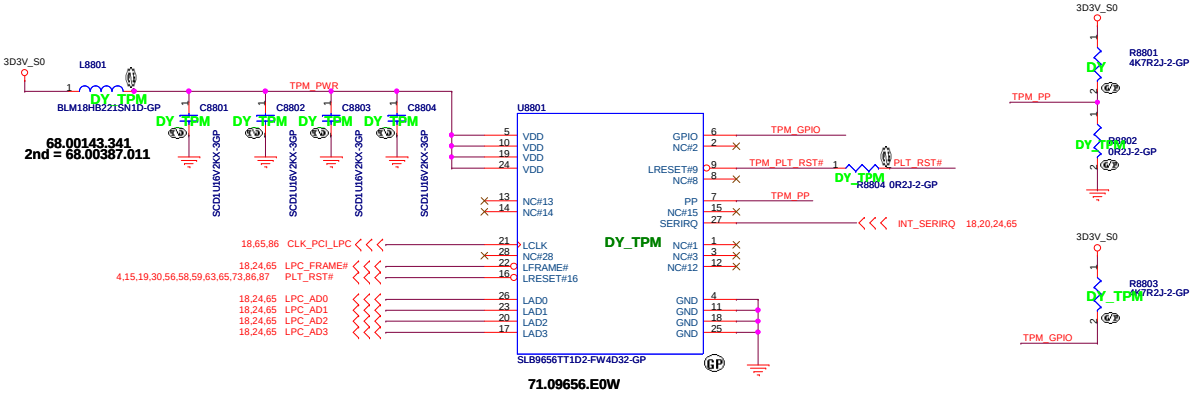

20130730 MV

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPM**

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Custom	2013 S-Series Shark Bay 14/15 17	
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<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Finger Print Conn

Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM5,6 (3/4)***

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14/15/17	A01

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<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
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<Variant Name>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

NCP3218 VGACORE25W

Size	Document Number	Rev
A2	2013 S-Series Shark Bay 14/15 17	1
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<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DISCRETE VGA POWER***

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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Shark Bay SV

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU XDP***

Size	Document Number	Rev
A3	**2013 S-Series Shark Bay 14 15 17**	1

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<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1

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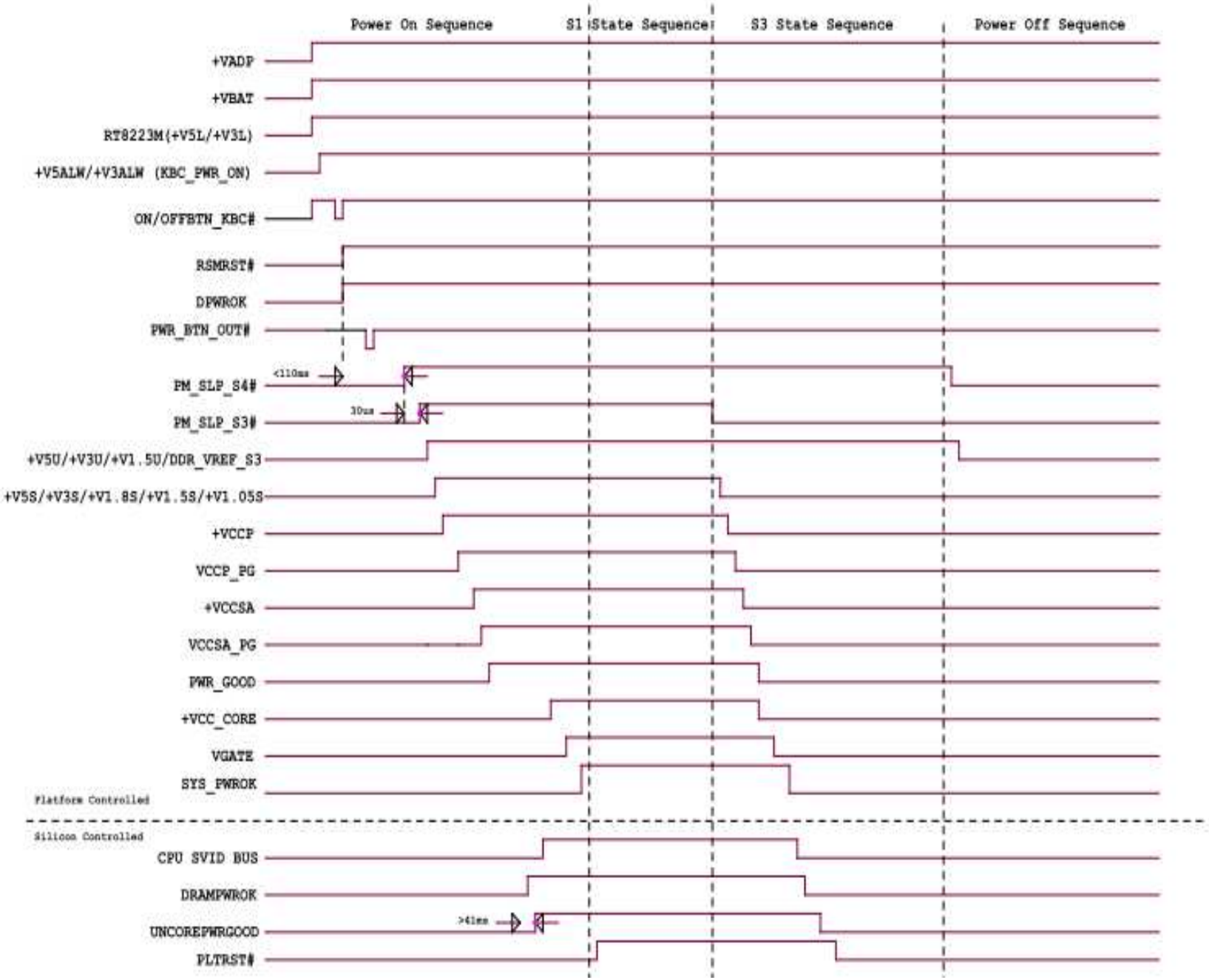
S-Series Power Sequence and Reset Signal Timing



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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Power Sequence***
Size: A3	Document Number: 2013 S-Series Shark Bay 14"15 17
Rev: 1.1	
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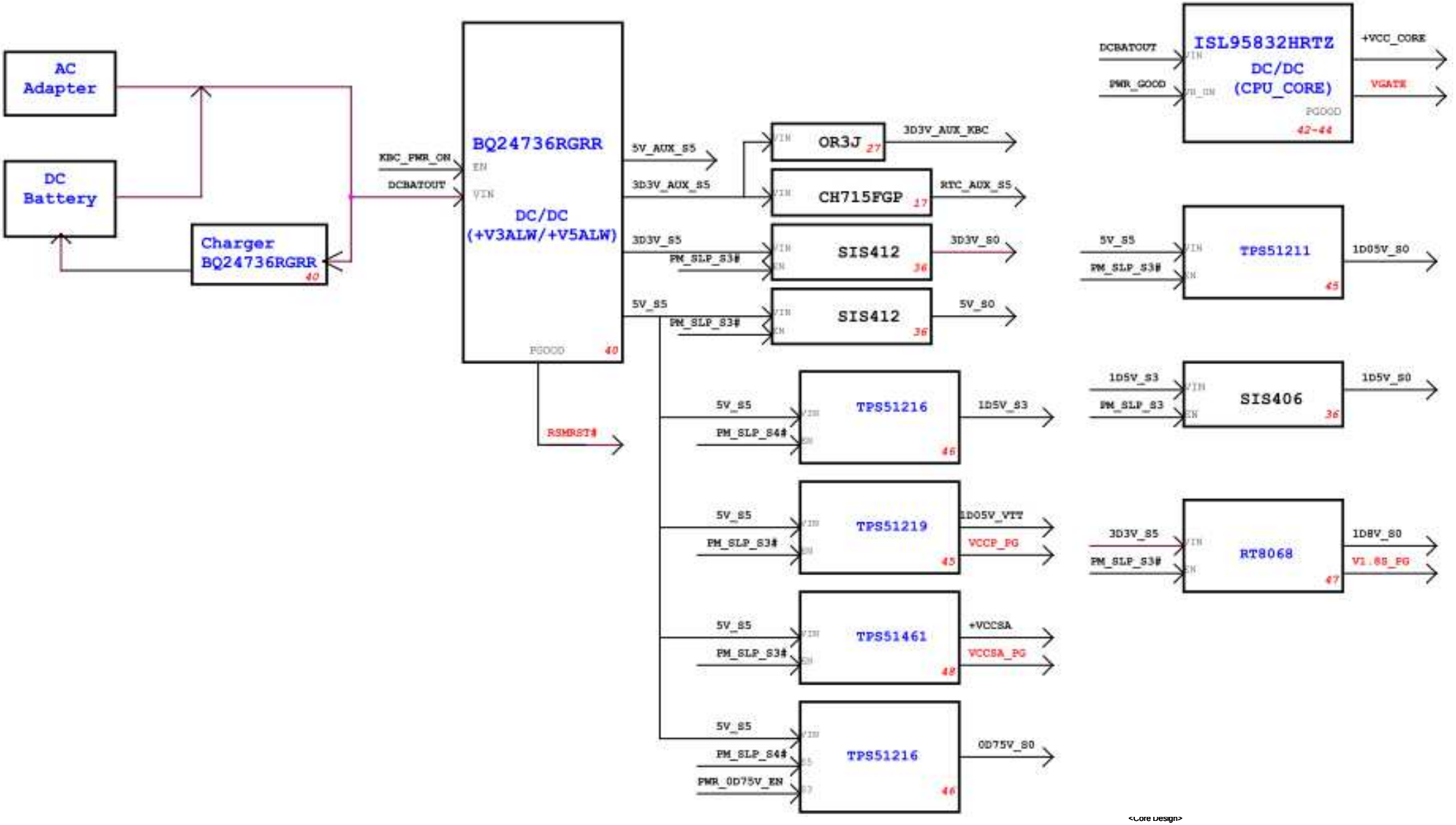
S-Series POWER BLOCK DIAGRAM



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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

Size	Document Number	Rev
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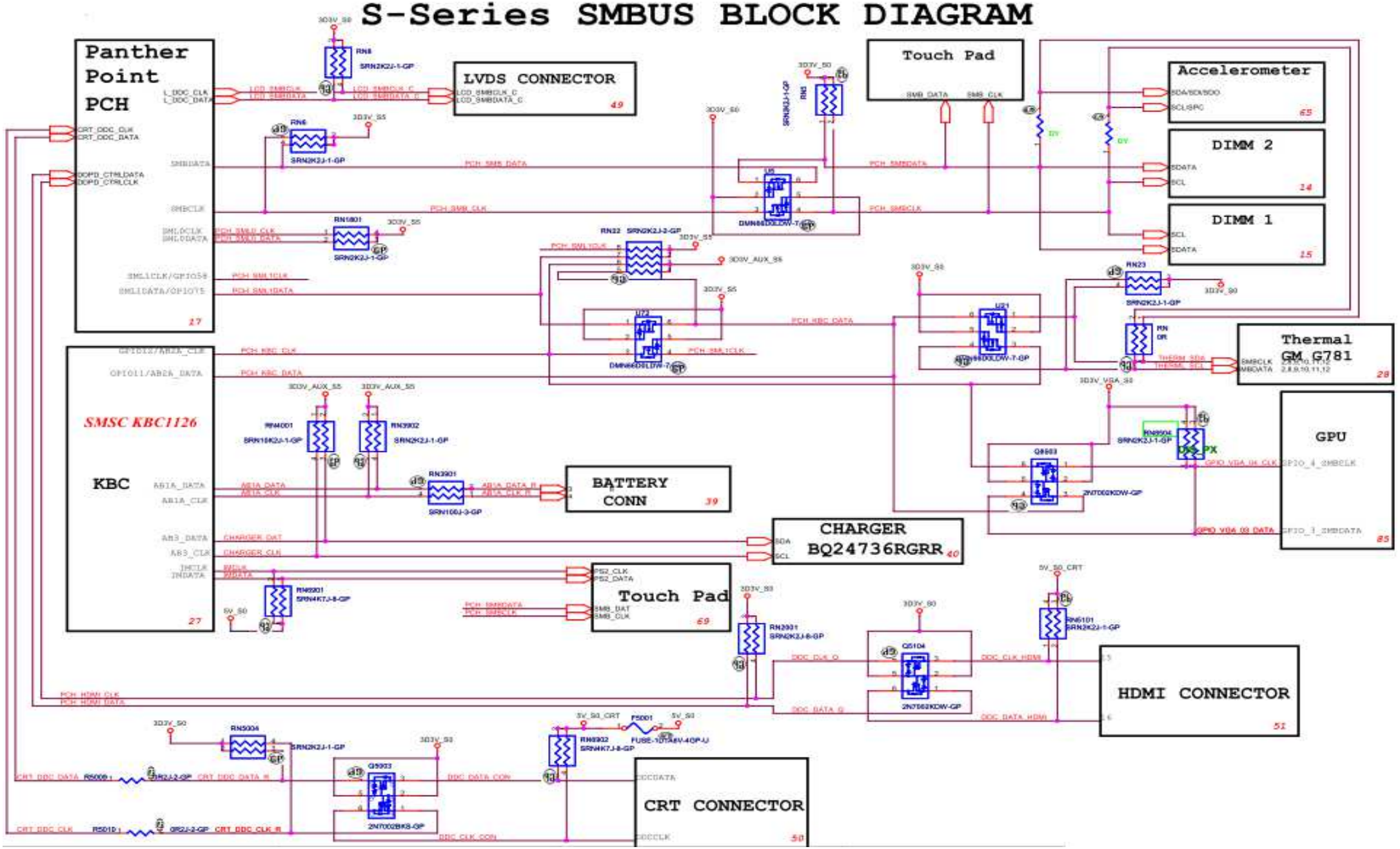
S-Series SMBUS BLOCK DIAGRAM



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SMBUS Block Diagram***

Size	Document Number	Rev
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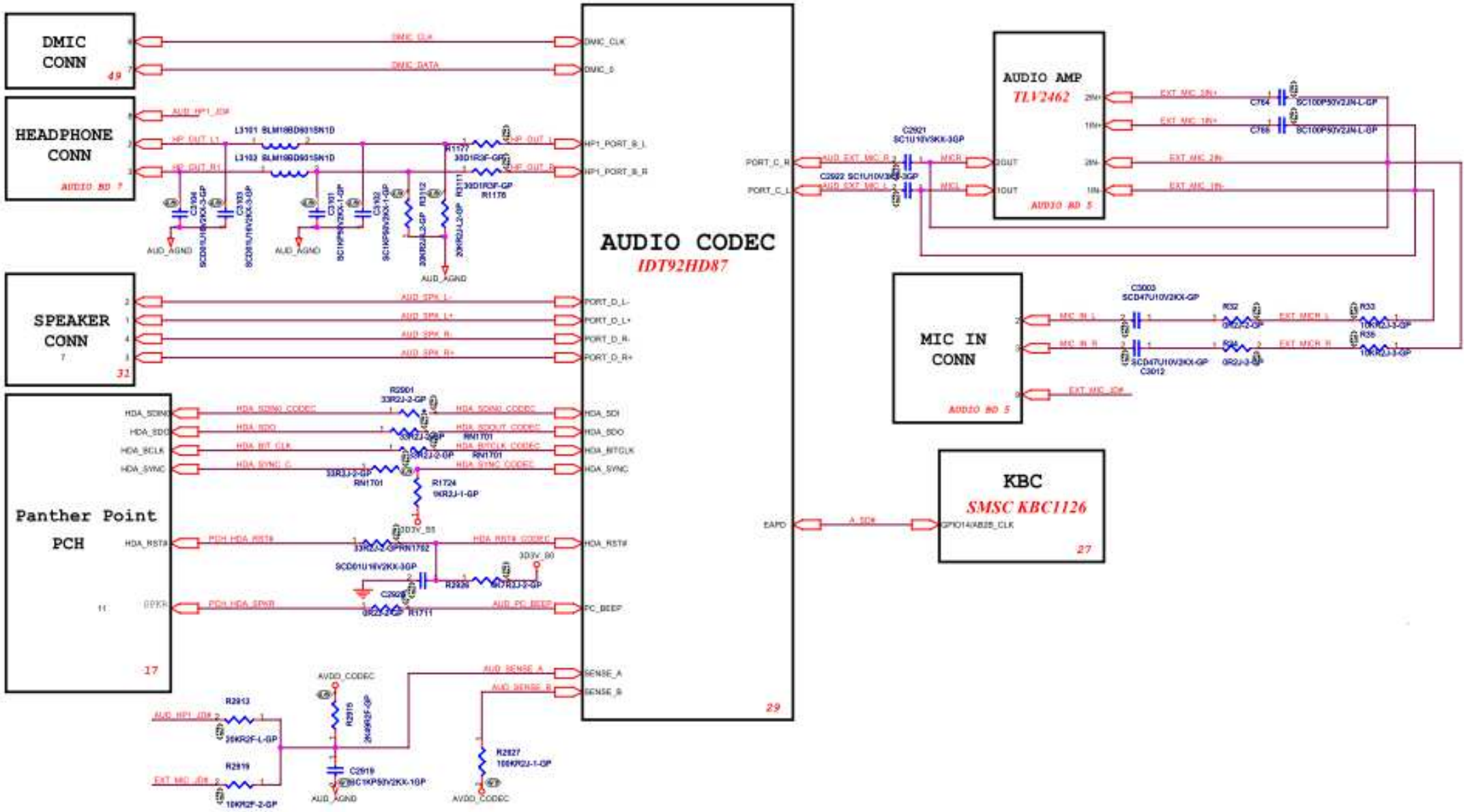
S-Series AUDIO BLOCK DIAGRAM



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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Thermal/Audio Block Diagram***	
Size: A3	Document Number: 2013 S-Series Shark Bay 14"15 17	Rev: 1
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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***mSATA***

Size	Document Number	Rev
A3	2013 S-Series Shark Bay 14 15 17	1.1

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